In Pursuit of Excellence	Course and Faculty Details	SESSION-2019-2020
		SEM- 3rd

Faculty Details

Name of the Faculty: Praveen Saini

Designation: Assistant Professor

Department: Computer Science & Engineering

Course Details

Name of the Programme: B.Tech. **Batch:** 2018-2022

Branch: CSE **Section:** A & C

Name of Subject: Computer Organization & Architecture

Subject Code: KCS-302

Category of Course: Core Subject

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Prof. & Head, CSE
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Moradabad-244001

In Pursuit of Excellence	**Index**	SESSION-2019-2020
		SEM- 3rd

Dr. Somesh Kumar
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Moradabad-244001

Vision of Institute

To develop industry ready professionals with values and ethics for global needs.

Mission of Institute

- To impart education through outcome based pedagogic principles.
- To provide conducive environment for personality development, training & entrepreneurial skills.
- To induct high professional ethics and accountability towards society in students.

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Vision of Department

To develop globally recognized computer science and engineering graduates with ethical values for need of software industries.

Mission of Department

1. To impart knowledge through well-defined instructional objectives in the field of computer science and engineering.
2. To provide a learning ambience for skills, innovation, leadership and overall personality development.
3. To inculcate professional ethics, teamwork and responsiveness towards society.

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Program Education Objectives

PEO 1 : The graduates will have entrepreneurial and employable skills in software industries, by adapting themselves in the corporate world by utilizing the defined instructional objectives learnt in the program.

PEO 2 : The graduates will engage in skill enhancement, that would help to work in their own area of interest, individually or in a team.

PEO 3 : The graduates will demonstrate ownership and responsiveness towards the profession and the society.

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Program Outcomes

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems.

2. Problem analysis: Identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety, and cultural, societal, and environmental considerations.

4. Conduct investigations of complex problems: Use research based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of information to provide valid conclusions.

5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling to complex engineering activities, with an understanding of the limitations.

6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. Communication: Communicate effectively on complex engineering activities with the engineering community and with the society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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After completing their graduation, students of Computer Science and Engineering will be able to -

PSO 1: Comprehend the core subjects of CSE and apply them to resolve domain specific tribulations.

PSO 2: Extrapolate the fundamental concepts in engineering and to apply latest technology with programming language skills to develop, test, implement and maintain software products.

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Moradabad Institute of Technology

Ramganga Vihar Phase – II, Moradabad

ACADEMIC CALENDAR

ODD Semester — Session: 2019 – 2020

S. No.	Particulars	Date	Responsibility
1.	**Time Table** (a) Display on Notice Boards (b) Distribution to concerned Teachers	 29 July 2019 29 July 2019	 O.C. Time – Table
2.	Distribution of class lists to teachers	29 July 2019	O.C. Class / DR
3.	**Registrations** (a) 3rd / 5th /7th Semester (b)List of unregistered students to various department (c) Notifying unregistered students for getting registered at the earliest (through class O.Cs. / Faculty)	 1,2,3 Aug.2019 20 Aug 2019 22 Aug 2019	 Concerned Teachers OS Academic Concerned HODs
4.	**Commencement of Classes** 3rd / 5th / 7th Semester	2,3,4 Aug.2019	Concerned Teachers
5.	Blow up submission to HODs	30 July 2019	Concerned Teachers
6.	Announcement of Test series dates	16Aug 2019	Dean Academics
7.	(a) Collection of Examination forms from University and announcement of date for availability of forms (b) Last date for submission of forms to office (c) Submission of forms to University	30 Aug 2019**	OS Academic to take timely action as per University directions.
8.	Procurement of stationary & materials for Test Series for full semester (a) Requirement (b) Actual Procurement	 31 Aug 2019 5 Sept 2019	Convener Test Series Committee O.S. Academics
9.	(a)Short attendance compilation and information to parents and undertaking format handed over to students (b)Collection of Short attendance undertaking	09 Sept 2019 11 Sept 2019	O.C. Class
10.	1st Test Series Thu, Fri, Sat	12, 13,14, Sept 2019	
	(a) Announcement of Test Series schedule, Invigilation Programme, Seating arrangement etc.	11 Sept 2019	Class Test Committee
	(b) After completion of Test Series- Evaluation of test copies & showing of copies to students	21 Sept 2019	Concerned Teachers
	(c) Submission of test copies in Nodal Centre (d) Report of poor performance of students to class OCs	25 Sept 2019 26 Sept 2019	Concerned Teachers Concerned Teachers
	(e)Short attendance compilation, display on notice board and information to parents	19 Oct 2019	O.C. Class
11.	2nd Test Series Wed, Thus, Fri	23,24, 25 Oct 2019	
	(a) Announcement of Test Series schedule, Invigilation Programme, seating arrangement etc	22 Oct 2019	Class Test Committee

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	(b) After completion of Test Series - Evaluation of test copies & showing of copies to students	02 Nov 2019	Concerned Teachers
	(c) Submission of test copies in Nodal Centre	04 Nov 2019	Concerned Teachers
	(d) Report of poor performance of students to class OCs	05 Nov 2019	Concerned Teachers
12.	Filling of student feedback forms for current semester	27 Nov 2019	Concerned HODs
13.	Requirement of additional Faculty (to be conveyed to Director) (for even semester)	30 Nov 2019	Concerned HODs
14.	(a) Floating the electives for even semester	26 Nov 2019	Concerned HODs
	(b) Last date for students choice	30 Nov 2019	
15.	Announcement of dues list and its last date for clearing dues (Current semester)	22 Oct 2019	Accounts/ OS Academic
16.	Date up to which final attendance is to be counted	29 Nov 2019	Concerned teachers
17.	Submission of consolidated list of shortage of attendance to Director and information to Parents	30 Nov 2019	Class O.Cs
18.	3rd Test Series Thu, Fri, Sat	28,29,30 Nov 2019	
	(a) Announcement of Test Series schedule, Invigilation Programme, Seating arrangement etc.	27 Nov 2019	Class Test Committee
	(b) After completion of Test Series- Evaluation of test copies & showing of copies to students	03 Dec2019	Concerned Teacher
	(c) Submission of test copies in Nodal Centre	04 Dec 2019	Concerned Teachers
	(d) Report of poor performance of students to class OCs	04 Dec 2019	Concerned Teachers
19.	**Submission of sessional marks:**		
	(a) Meeting of Dean Academics, , all HODs and Director regarding attendance and performance of students.	04 Dec 2019	Dean Academics
	(b) Checking of Teachers' Records by HODs	05 Dec 2019	Concerned HODs
	(c) Finalization of sessional marks	05 Dec 2019	Concerned Teachers
	(d) Submission of Award list after final checking and uploading to OS Academics for further necessary action	As per date announced by AKTU	HODs Concerned Teachers
20.	**Theory Examinations:** (a) Collection of Admit Cards / Roll Nos. from University (b) Preparation of Roll lists (c) Collection of stationery such as copies, practical copies drawing sheets, graph paper etc. from University. (c) Procurement of stationery and other materials locally as necessary.	As per AKTU schedule	OS Academics to take appropriate actions as per University directions.
21.	**Practical Examinations:**		
	(a) Appointment of Internal Examiners	As per AKTU schedule	Concerned HODs
	(b) Obtaining list of panel of External Examiners from AKTU & preparation of schedule of practical examination.	3 days before the practical exam schedule	Concerned HODs
	(d) Dispatch of letters/contacting the external examiners	As per AKTU schedule	OS Academics
		Within 2 days of list obtained from AKTU	HODs and concerned teachers

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22.	**Preparation for Even Semester** (a) Load Distribution by Department (b) Submission to O.C. Time-Table (c) Display of Time Table on Notice Board	10 Dec 2019 12 Dec 2019 18 Jan 2020	Concerned Coordinators O.C. Time Table
23.	Registration for Even semester [2019 – 20]	To be announced**	OS Academic
24.	Announcement of Academic calendar for Even semester [2019 – 20]	5 Days before the start of Even sem.	Dean Academics

**May be revised as per AKTU Schedule.

27.7.2019

Dean Academics

Director

Copy to:

1. Chairman	2. Secretary	3. P.A. to Director for Director's folder
4. All HODs	5. DOSW	6. Controller Examination
7. Associate Dean Academics	8. Registrar	9. All Faculty Members through HODs
10. O.S. Academics	11. A.S. Examinations	12. Accounts Section
13. T & P Cell	14. Librarian	15. Convener Test Series/ O.C. Time Table

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MORADABAD INSTITUTE OF TECHNOLOGY, MORADABAD

Ram Ganga Vihar Phase-II Moradabad (U.P.)
Approved by AICTE and Affiliated to Dr. A. P. J. Abdul Kalam Technical University, Lucknow
Website: http://mitmoradabad.edu.in

Department Academic Calendar, Odd Semester, Session (2019 – 2020)

VISION

To develop globally recognized computer science and engineering graduates with ethical values for need of software industries.

MISSION

M1: To impart knowledge through well defined instructional objectives in the field of computer science and engineering.
M2: To provide a learning ambience for skills, innovation, leadership and overall personality development.
M3: To inculcate professional ethics, teamwork and responsiveness towards society.

JULY-2019

Su	M	T	W	Th	F	S
	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31			

AUGUST-2019

Su	M	T	W	Th	F	S
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31

SEPTEMBER-2019

Su	M	T	W	Th	F	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30					

OCTOBER-2019

Su	M	T	W	Th	F	S
		1	2	3	4	5
6	7	8	9	10	11	12
13	14	15	16	17	18	19
20	21	22	23	24	25	26
27	28	29	30	31		

NOVEMBER-2019

Su	M	T	W	Th	F	S
					1	2
3	4	5	6	7	8	9
10	11	12	13	14	15	16
17	18	19	20	21	22	23
24	25	26	27	28	29	30

DECEMBER-2019

Su	M	T	W	Th	F	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

A	Time Table Display on Notice Boards
B	Blow Up Submission to HODs
C	3rd /5th /7th semester registration
D	Commencement of Classes of 3rd /5th /7th semester
E	Eid Ul Zuha
F	Independence day and Rakshabandhan
G	Event 'Kanha ki Matki' by CSSS
H	Krishna Janmashtami
I	Short Attendance compilation and information to parents
J	Moharram
K	1st Test Series
L	Submission of Test copies in Nodal Center
M	Event 'ArtShala' by CSSS
N	Gandhi Jayanti
O	Expert Lecture on DevSecOps by Mr Kavish Baghel, Thoughts2Binary Gurugram
P	Maha Navmi
Q	Dussehra
R	Maharishi Valmiki Jayanti
S	Event 'KuruShetra' by CSSS
T	Short Attendance compilation and information to parents
U	2nd Test Series
V	Mid Semester Break
W	Submission of Test copies in Nodal Center
X	Eid-e-eMilad
Y	Guru Nanak Birthday
Z	Event 'Coder 6.0' by CSSS
AA	Floating the electives for even sem (2019-20)
AB	Filling of Student Feedback form for current Semester
AC	3rd Test Series
AD	Submission of consolidated list of shortage of attendance to director and information to parents
AE	Submission of Test copies in Nodal Center
AF	Submission of Sessional marks
AG	Christmas

Month	Dates of Teaching Days (2nd, 3rd & 4th Year)	No. of Teaching Days	No. of Lecture Hours
Jul-19		NA	91*6=546
Aug-19	3,5,6,7,8,9,10,13,14,16,17,19,20,21,22,24,26,27,28,29,30,31	22	
Sep-19	2,3,4,5,6,7,9,11,16,17,18,19,120,21,23,24,25,26,27,28,30	21	
Oct-19	1,3,4,5,9,10,11,12,14,15,16,17,18,19,21,22,31	17	
Nov-19	1,2,4,5,6,7,8,9,11,13,14,15,16,18,19,20,21,22,23,25,26,27	22	
		82	
	Sessional Examinations	09	
	Total	**91**	**546**

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B.TECH (COMPUTER SCIENCE AND ENGINEERING)

SEMESTER- III

Sl. No.	Subject Codes	Subject	Periods			Evaluation Scheme				End Semester		Total	Credit
			L	T	P	CT	TA	Total	PS	TE	PE		
1	KOE031-38/ KAS302	Engineering Science Course/Maths IV	3	1	0	30	20	50	-	100		150	4
2	KAS301/ KVE 301	Technical Communication/Universal Human values	2 3	1 0	0 0	30	20	50		100		150	3
3	KCS301	Data Structure	3	1	0	30	20	50		100		150	4
4	KCS302	Computer Organization and Architecture	3	1	0	30	20	50		100		150	4
5	KCS303	Discrete Structures & Theory of Logic	3	0	0	30	20	50		100		150	3
6	KCS351	Data Structures Using C Lab	0	0	2				25		25	50	1
7	KCS352	Computer Organization Lab	0	0	2				25		25	50	1
8	KCS353	Discrete Structure & Logic Lab	0	0	2				25		25	50	1
9	KCS354	Mini Project or Internship Assessment*	0	0	2			50				50	1
10	KNC301/ KNC302	Computer System Security/Python Programming	2	0	0	15	10	25		50			0
11		MOOCs (Essential for Hons. Degree)											
		Total										**950**	**22**

*The Mini Project or internship (3-4 weeks) conducted during summer break after II semester and will be assessed during III semester.

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In Pursuit of Excellence	Course Syllabus as per University	SESSION-2019-2020 SEM- 3rd

KCS302 Computer Organization & Architecture

DETAILED SYLLABUS		3-1-0
Unit	Topic	Proposed Lecture
I	**Introduction**: Functional units of digital system and their interconnections, buses, bus architecture, types of buses and bus arbitration. Register, bus and memory transfer. Processor organization, general registers organization, stack organization and addressing modes.	08
II	**Arithmetic and logic unit:** Look ahead carries adders. Multiplication: Signed operand multiplication, Booths algorithm and array multiplier. Division and logic operations. Floating point arithmetic operation, Arithmetic & logic unit design. IEEE Standard for Floating Point Numbers	08
III	**Control Unit:** Instruction types, formats, instruction cycles and sub cycles (fetch and execute etc), micro operations, execution of a complete instruction. Program Control, Reduced Instruction Set Computer, Pipelining. Hardwire and micro programmed control: micro programme sequencing, concept of horizontal and vertical microprogramming.	08
IV	**Memory:** Basic concept and hierarchy, semiconductor RAM memories, 2D & 2 1/2D memory organization. ROM memories. Cache memories: concept and design issues & performance, address mapping and replacement Auxiliary memories: magnetic disk, magnetic tape and optical disks Virtual memory: concept implementation.	08
V	**Input / Output**: Peripheral devices, I/O interface, I/O ports, Interrupts: interrupt hardware, types of interrupts and exceptions. Modes of Data Transfer: Programmed I/O, interrupt initiated I/O and Direct Memory Access., I/O channels and processors. Serial Communication: Synchronous & asynchronous communication, standard communication interfaces.	08

Text books:

1. Computer System Architecture - M. Mano
2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky Computer Organization, McGraw-Hill, Fifth Edition, Reprint 2012
3. John P. Hayes, Computer Architecture and Organization, Tata McGraw Hill, Third Edition, 1998. Reference books
4. William Stallings, Computer Organization and Architecture-Designing for Performance, Pearson Education, Seventh edition, 2006.
5. Behrooz Parahami, "Computer Architecture", Oxford University Press, Eighth Impression, 2011.
6. David A. Patterson and John L. Hennessy, "Computer Architecture-A Quantitative Approach", Elsevier, a division of reed India Private Limited, Fifth edition, 2012
7. Structured Computer Organization, Tannenbaum(PHI)

Computer Organization Lab

1. Implementing HALF ADDER, FULL ADDER using basic logic gates
2. Implementing Binary -to -Gray, Gray -to -Binary code conversions.
3. Implementing 3-8 line DECODER.
4. Implementing 4x1 and 8x1 MULTIPLEXERS.
5. Verify the excitation tables of various FLIP-FLOPS.
6. Design of an 8-bit Input/ Output system with four 8-bit Internal Registers.
7. Design of an 8-bit ARITHMETIC LOGIC UNIT.
8. Design the data path of a computer from its register transfer language description.
9. Design the control unit of a computer using either hardwiring or microprogramming based on its register transfer language description.
10. Implement a simple instruction set computer with a control unit and a data path.

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Syllabus

Pre-requisites:

Logic Design.

KCS302 Computer Organization & Architecture

Unit I

Review: ***Brief review of Digital Computer System***

Introduction: Functional units of digital system and their interconnections, buses, bus architecture, types of buses and bus arbitration.

Register, bus and memory transfer. Processor organization, general registers organization, stack organization and addressing modes.

Beyond: ***Generation of Computers, Von-Neumann Architecture, Overview of Stack as a data structure***

Unit II

Review: Number System and operations performed on them

Arithmetic and logic unit: Look ahead carries adders. Multiplication: Signed operand multiplication, Booths algorithm and array multiplier. Division and logic operations.

Floating point arithmetic operation, Arithmetic & logic unit design. IEEE Standard for Floating Point Numbers

Beyond: ***Overview of Combinational logic circuits***

Unit III

Review: Basic Understanding of Control Unit and its working

Control Unit: Instruction types, formats, instruction cycles and sub cycles (fetch and execute etc), micro operations, execution of a complete instruction. Program Control,

Bridging: Instruction Set Architecture

Reduced Instruction Set Computer, Pipelining. Hardwire and micro programmed control: micro programme sequencing, concept of horizontal and vertical microprogramming.

Beyond: ***Overview of Sequential logic Circuits***

Unit IV

Memory: Basic concept and hierarchy, semiconductor RAM memories, 2D & 2 1/2D memory organization. ROM memories. Cache memories: concept and design issues & performance, address mapping and replacement Auxiliary memories: magnetic disk, magnetic tape and optical disks

Virtual memory: concept implementation

Unit V

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Input / Output: Peripheral devices, I/O interface, I/O ports, Interrupts: interrupt hardware, types of interrupts and exceptions. Modes of Data Transfer: Programmed I/O, interrupt initiated I/O and Direct Memory Access., I/O channels and processors. Serial Communication: Synchronous asynchronous communication, standard communication interfaces.

References:

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky Computer Organization, McGraw-Hill, Fifth Edition, Reprint 2012

2. Structured Computer Organization, Tannenbaum(PHI)

3. William Stallings, Computer Organization and Architecture-Designing for Performance, Pearson Education, Seventh edition, 2006.

Additional References:

4. John P. Hayes, Computer Architecture and Organization, Tata McGraw Hill, Third Edition, 1998. Reference books

5. Behrooz Parahami, "Computer Architecture", Oxford University Press, Eighth Impression, 2011.

6. David A. Patterson and John L. Hennessy, "Computer Architecture-A Quantitative Approach", Elsevier, a division of reed India Private Limited, Fifth edition, 2012

Text Books:

7. Computer System Architecture - M. Mano

Web References:

8. https://nptel.ac.in/courses/106/105/106105163/

9. http://csillustrated.berkeley.edu/PDFs/handouts/cache-3-associativity-handout.pdf

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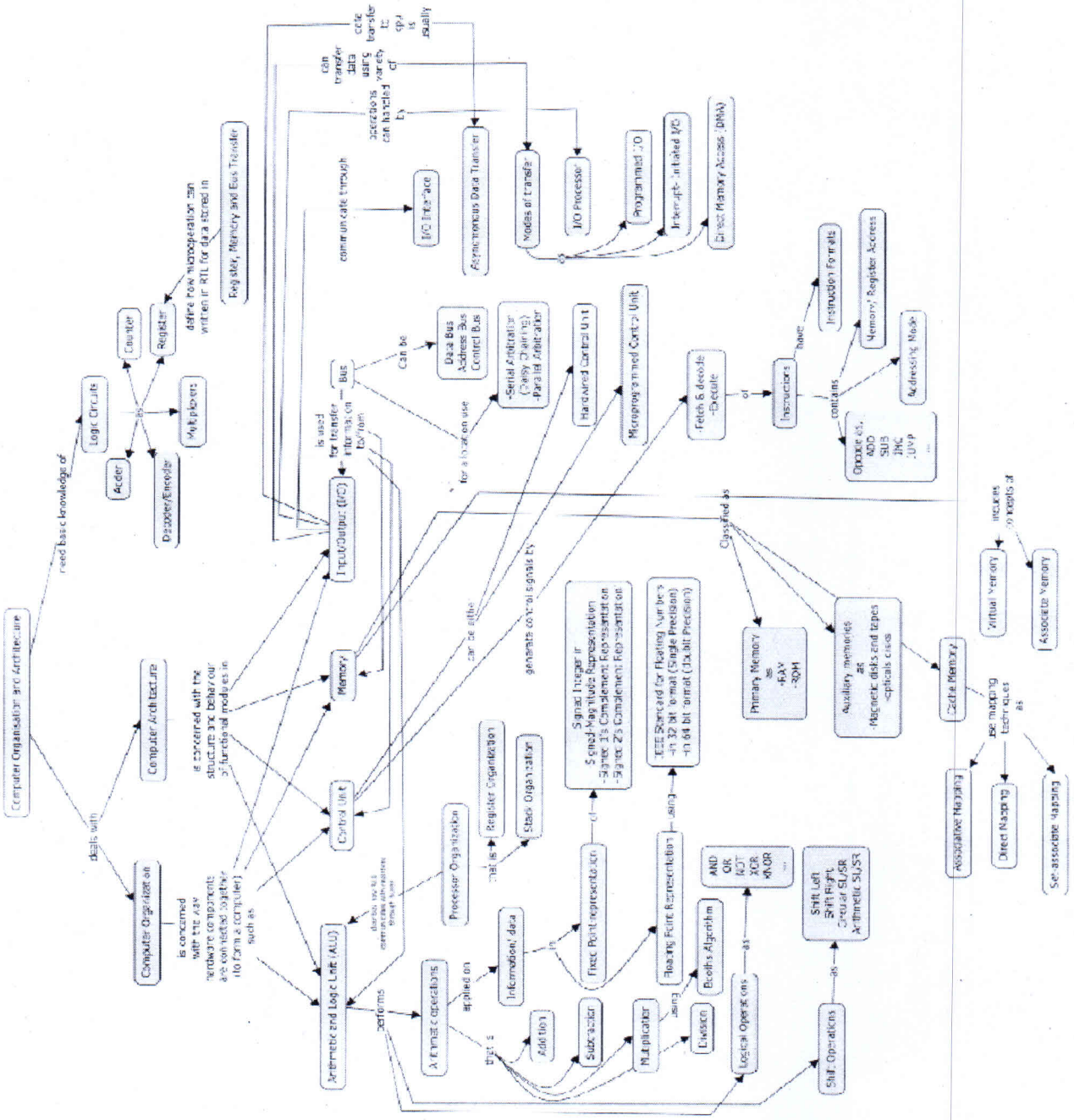
In Pursuit of Excellence	**Concept Map**	SESSION-2019-2020 SEM- 3rd

KCS302 Computer Organization & Architecture



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In Pursuit of Excellence	**Course Outcomes**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization and Architecture		
Course Outcomes (COs) as per the requirement of a program-		**Bloom's Knowledge Level**
At the end of course, the student will be able to		
CO1	Define the basic organization and design of digital computer system and its operation	Understand
CO2	Explain the design of arithmetic & logic unit and algorithms for the fixed point and floating-point arithmetic operations.	Apply
CO3	Illustrate control unit design techniques and the concept of Pipelining	Understand
CO4	Explain the hierarchical memory system, cache memories and virtual memory	Understand
CO5	Illustrate different ways of communicating with I/O devices and standard I/O interfaces and their functioning	Understand

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In Pursuit of Excellence	**Course Delivery Method**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Delivery Methods:

Coverage of
Unit 1 by: - Chalk & Talk, Tutorials, solving numerical, assignments
Unit 2 by: - Chalk & Talk, Tutorials, solving numerical, Simulation Software, assignments
Unit 3 by: - Chalk & Talk, Tutorials, solving numerical, Simulation Software, assignments
Unit 4 by: - Chalk & Talk, Tutorials, solving numerical, assignments
Unit 5 by: - Chalk & Talk, Tutorials, assignment.

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In Pursuit of Excellence	**Mapping**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Mapping of Course Outcomes with POs & PSOs:

Sr. No	Course Outcome	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO 2
1	CO 1	3									2			3	
2	CO 2	3	2	3	3	2					2		3	3	
3	CO 3	3		2		2					2		2	3	
4	CO 4	3				2					2			3	
5	CO 5	3									2			3	

*3= High *2= Medium

CO1. Define the basic organization and design of digital computer system and its operation

CO2. Explain the design of arithmetic & logic unit and algorithms for the fixed point and floating-point arithmetic operations.

CO3. Illustrate control unit design techniques and the concept of Pipelining

CO4. Explain the hierarchical memory system, cache memories and virtual memory

CO5. Illustrate different ways of communicating with I/O devices and standard I/O interfaces and their functioning

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In Pursuit of Excellence	**Time Table**	SESSION-2019-2020 SEM- 3rd

Day	9.00AM-10.00 AM	10.00AM-11.00 AM	11.00AM-12.00 NOON	12.00 AM-01.00 PM	01.00 PM-2.00 PM	2.00PM - 3.00 PM	3.00PM-4.00 PM	4.00PM-5.00 PM
MON	KCS-352 3rd A2 B-117		KCS-302 (L) 3rd A B-311		L U N C H		KCS-352 3rd B2 B-117	
TUE				KCS-302 (T) 3rd A2 B-317		KCS-352 3rd A1 B-117		
WED				KCS-302 (T) 3rd A3 B-319				
THU	KCS-302 (L) 3rd A B-311		KCS-302 (T) 3rd C3 B-319	KCS-302 (L) 3rd C B-323			KCS-302 (T) 3rd C2 B-311	
FRI		KCS-302 (L) 3rd C B-323				KCS-302 (T) 3rd C1 B-316		
SAT	KCS-302 (T) 3rd A1 B-316	KCS-302 (L) 3rd A B-311		KCS-302 (L) 3rd C B-318				

SUB. CODE	SUBJECT
KCS-302	Computer Organization & Architecture
KCS-352	Computer Organization Lab

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In Pursuit of Excellence	**Lecture Plan & Course Coverage**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Total Period: 40 **Section A**

Sr. No.	No. of Periods	Topics/Sub Topics	Reference Books	CO Covered	Planned Date	Coverage Date	Sign
1.	1	**Topic(s) Beyond Syllabus: Von Neumann Architecture, Generation of Computers**	R1	CO1	03/08/2019	03/08/2019	
2.	1	Introduction: Functional units of digital system and their interconnections	R1	CO1	05/08/2019	05/08/2019	
3.	2	buses, bus architecture, types of buses	R1	CO1	08/08/2019 10/08/2019	08/08/2019 17/08/2019	
4.	1	bus arbitration.	R1	CO1	17/08/2019	19/08/2019	
5.	1	Register bus and memory transfer	T7	CO1	19/08/2019	22/08/2019	
6.	2	Processor organization, general register organization, stack organization	T7	CO1	22/08/2019 24/08/2019	26/08/2019 29/08/2019	
7.	1	Addressing modes, **Topic(s) Beyond Syllabus:** Overview of Stack as a data structure	R1	CO1	26/08/2019	31/08/2019	
8.	2	**Topic(s) Beyond Syllabus:** Overview of Combinational logic circuits, Arithmetic and logic unit: Look ahead carry adders	R1	CO2	29/08/2019 31/08/2019	02/09/2019 03/09/2019 05/09/2019	
9.	1	Multiplication: Signed operand multiplication	T7, R1	CO2	02/09/2019	07/09/2019	
10.	1	Booths algorithm and array multiplier	R1	CO2	05/09/2019	09/09/2019	

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11.	2	Division, logic operations and Floating-point arithmetic operation	R1	CO2	07/09/2019 09/09/2019	16/09/2019 19/09/2019	
13.	2	Arithmetic & logic unit design.	R3, R1	CO2	16/09/2019 19/09/2019	20/09/2019 23/09/2019	
14.	1	Control Unit: Instruction types, formats	R1, T7	CO3	21/09/2019	26/09/2019	
15.	2	Instruction cycles and sub cycles (fetch, execute etc), micro-operations, Execution of a complete instruction	R1,T7	CO3	23/09/2019 26/09/2019	28/09/2019 30/09/2019	
16.	2	Program Control, Reduced Instruction Set Computer	T7	CO3	28/09/2019 30/09/2019	01/10/2019 03/10/2019	
17.	1	Pipelining	T7, R1	CO3	03/10/2019	05/10/2019	
18.	1	Hardwire and micro programmed control: Micro-programmed sequencing	R1	CO3	05/10/2019	10/10/2019	
19.	1	Concept of horizontal and vertical microprogramming **Topic(s) Beyond Syllabus:** Overview of Sequential logic Circuits	R1	CO3	10/10/2019	12/10/2019	
20.	1	Memory: Basic concept and hierarchy, semiconductor RAM memories	T7	CO4	12/10/2019	14/10/2019	
21.	1	2D & 2.5 D memory organization	T7	CO4	14/10/2019	17/10/2019	
22.	1	ROM memories	T7	CO4	17/10/2019	19/10/2019	
23.	1	Cache memories: concept and design issues & performance	T7, W9	CO4	19/10/2019	31/10/2019	
24.	1	address mapping and replacement	T7	CO4	31/10/2019	02/11/2019 04/11/2019	
25.	2	Auxiliary memories: magnetic disk, magnetic tape and optical disks	T7	CO4	02/11/2019 04/11/2019	05/11/2019 07/11/2019	

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26.	1	Virtual memory: concept implementation	T7	CO4	07/11/2019	13/11/2019	
27.	1	Input / Output: Peripheral devices, I/O interface, I/O ports	T7	CO5	09/11/2019	14/11/2019	
28.	1	Interrupts: interrupt hardware, types of interrupts and exceptions	T7	CO5	11/11/2019	15/11/2019	
29.	2	Modes of Data Transfer: Programmed I/O, interruptinitiated I/O	T7	CO5	14/11/2019 16/11/2019	15/11/2019 16/11/2019	
30.	1	Direct Memory Access	T7	CO5	18/11/2019	18/11/2019 21/11/2019	
31.	1	I/O channels and processors	T7	CO5	21/11/2019	22/11/2019	
32.	1	Serial Communication: Synchronous & asynchronous communication, standard communication interfaces	T7	CO5	23/11/2019	23/11/2019	

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KCS302: Computer Organization & Architecture

Total Period: 40 **Section C**

Sr. No.	No. of Periods	Topics/Sub Topics	Reference Books	CO Covered	Planned Date	Coverage Date	Sign
1.	1	**Topic(s) Beyond Syllabus: Von Neumann Architecture, Generation of Computers**	R1	CO1	02/08/2019	02/08/2019	
2.	1	Introduction: Functional units of digital system and their interconnections	R1	CO1	03/08/2019	03/08/2019	
3.	2	buses, bus architecture, types of buses	R1	CO1	08/08/2019 09/08/2019	08/08/2019 09/08/2019	
4.	1	bus arbitration.	R1	CO1	10/08/2019	16/08/2019	
5.	1	Register bus and memory transfer	T7	CO1	16/08/2019	17/08/2019	
6.	2	Processor organization, general register organization, stack organization	T7	CO1	17/08/2019 22/08/2019	22/08/2019 23/08/2019	
7.	1	Addressing modes, **Topic(s) Beyond Syllabus:** Overview of Stack as a data structure	R1	CO1	24/08/2019	29/08/2019	
8.	2	**Topic(s) Beyond Syllabus:** Overview of Combinational logic circuits, Arithmetic and logic unit: Look ahead carry adders	R1	CO2	29/08/2019 30/08/2019	30/08/2019 05/09/2019 06/09/2019	
9.	1	Multiplication: Signed operand multiplication	T7,R1	CO2	31/08/2019	07/09/2019	
10.	1	Booths algorithm and array multiplier	R1	CO2	05/09/2019	09/09/2019	
11.	2	Division, logic operations and Floating point arithmetic operation	R1	CO2	06/09/2019 07/09/2019	19/09/2019 20/09/2019	

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13.	2	Arithmetic & logic unit design.	R3, R1	CO2	19/09/2019 20/09/2019	26/09/2019 27/09/2019	
14.	1	Control Unit: Instruction types, formats	R1,T7	CO3	21/09/2019	28/09/2019	
15.	2	Instruction cycles and sub cycles (fetch, execute etc), micro-operations, Execution of a complete instruction	R1,T7	CO3	26/09/2019 27/09/2019	03/10/2019 04/10/2019	
16.	2	Program Control, Reduced Instruction Set Computer	T7	CO3	28/09/2019 03/10/2019	05/10/2019 10/10/2019	
17.	1	Pipelining	T7, R1	CO3	04/10/2019	11/10/2019	
18.	1	Hardwire and micro programmed control: Micro-programmed sequencing	R1	CO3	05/10/2019	12/10/2019	
19.	1	Concept of horizontal and vertical microprogramming **Topic(s) Beyond Syllabus:** Overview of Sequential logic Circuits	R1	CO3	10/10/2019	17/10/2019	
20.	1	Memory: Basic concept and hierarchy, semiconductor RAM memories	T7	CO4	11/10/2019	31/10/2019	
21.	1	2D & 2.5 D memory organization	T7	CO4	12/10/2019	01/11/2019	
22.	1	ROM memories	T7	CO4	17/10/2019	02/11/2019	
23.	1	Cache memories: concept and design issues & performance	T7	CO4	18/10/2019	07/11/2019	
24.	1	address mapping and replacement	T7	CO4	19/10/2019	08/11/2019	
25.	2	Auxiliary memories: magnetic disk, magnetic tape and optical disks	T7	CO4	31/10/2019 01/11/2019	14/11/2019 14/11/2019	
26.	1	Virtual memory: concept implementation **Topic(s) Beyond Syllabus:** Building of Basic memory element -Flip-flops	T7	CO4	02/11/2019	15/11/2019	

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27.	1	Input / Output: Peripheral devices, I/O interface, I/O ports	T7	CO5	07/11/2019	16/11/2019	
28.	1	Interrupts: interrupt hardware, types of interrupts and exceptions	T7	CO5	08/11/2019	19/11/2019	
29.	2	Modes of Data Transfer: Programmed I/O, interruptinitiated I/O	T7	CO5	09/11/2019 14/11/2019	21/11/2019	
30.	1	Direct Memory Access	T7	CO5	15/11/2019	22/11/2019	
31.	1	I/O channels and processors	T7	CO5	16/11/2019	23/11/2019	
32.	1	Serial Communication: Synchronous & asynchronous communication, standard communication interfaces	T7	CO5	21/11/2019	23/11/2019	

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In Pursuit of Excellence	**Tutorial-1**	SESSION-2019-2020 SEM-3rd

KCS302: Computer Organization & Architecture

Sr. No.	No. of Periods	Topics/Sub Topics	Coverage Date						Sign
			Section A			Section B			
			A1	A2	A3	C1	C2	C3	
1.	1	Introduction to Computer Organization & Architecture, 2's complement and Subtraction	03/08/2019	06/08/2019	07/08/2019	09/09/2019	03/08/2019	08/08/2019	

CO1

1. **What do you mean by Computer Organization and Computer Architecture.**
2. **Explain in detail about Generation of computers.**
3. **Convert the following decimal numbers to binary using 6-bit 2's complement representation.**
   - i. -16_{10}
   - ii. 13_{10}
   - iii. -3_{10}
   - iv. -10_{10}
   - v. 26_{10}
   - vi. -31_{10}

[Answer – i. 110000_2 ii. 001101_2 iii. 111101_2 iv. 110110_2 v. 011010_2 vi. 100001_2

4. **Solve each of the following 4-bit subtraction problems using 2's complement representation.**

a. $00110_2 - 00101_2$
b. $01100_2 - 01010_2$
c. $00100_2 - 00101_2$
d. $01001_2 - 01011_2$
e. $00011_2 - 01100_2$
f. $00110_2 - 01001_2$

[Answer – i. 00001_2 ii. 00010_2 iii. 11110_2 iv. 11101_2 v. 10110_2 vi. 11100_2

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In Pursuit of Excellence	**Tutorial-2**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Sr. No.	No. of Periods	Topics/Sub Topics	Coverage Date						Sign
			Section A			Section B			
			A1	A2	A3	C1	C2	C3	
1.	1	**Von-Neumann Architecture** , Functional Components of Digital Computer and its Interconnection, Implementation of Bus using Multiplexer	17/08/2019	13/09/19	14/08/2019	16/08/2019	22/08/2019	22/08/2019	

CO1

1. What is typical digital computer? Explain it with the help of block diagram and its various parts.
2. What do you understand by Von-Neumann Architecture. Why it is important?
3. Explain the interconnection between processor and Memory.
4. What do you understand by Bus. Explain with its types.
5. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is conducted with multiplexers.
    a. How many selection inputs are there in each multiplexer
    b. What size of multiplexers are needed?
    c. How many multiplexers are there in the bus?
6. What has to be done to the bus system implemented using Multiplexer to be able to transfer information from any register to any other register? Specifically, show the connections that must be included to provide a path from the outputs of register C to the inputs of register A.

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In Pursuit of Excellence	**Tutorial-3**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Sr. No.	No. of Periods	Topics/Sub Topics	Coverage Date						Sign
			Section A			Section B			
			A1	A2	A3	C1	C2	C3	
1.	1	Three State Buffer, Registers	31/08/2019	20/09/2019	21/09/2019	23/08/2019	29/08/2019	29/08/2019	

CO1

1. Draw a diagram of bus system using three state buffers and a decoder for four registers each of four bits.
2. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with three-state buffer.
   a. How many decoders are required for each bit?
   b. What will be the size of each decoder?
   c. In total, how many three-state buffers are used?
3. Show the block diagram of the hardware that implements the following register transfer statement

   yT_2: R2←R1, R1←R2
4. Represent the following conditional control statement by two register transfer statements with control functions.

   If (P=1) then (R1 ← R2) else if (Q = 1) then (R1 ← R3)
5. The following transfer statements specify a memory operation. Explain the memory operation in each case:

   (i) R2 ←M [AR]
   (ii) M [AR] ←R3
   (iii) R5 ←M [R5]
6. Show the hardware that implements the following statement:

   $xyT_0 + T_1 + y'T_2$: $AR \leftarrow AR + 1$

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In Pursuit of Excellence	**Tutorial-4**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Sr. No.	No. of Periods	Topics/Sub Topics	Coverage Date						Sign
			Section A			Section B			
			A1	A2	A3	C1	C2	C3	
1.	1	Arithmetic Micro-operations, Logical Micro-operations.	07/09/2019	27/08/2019	28/08/2019	30/08/2019	05/09/2019	05/09/2019	

CO1

1. The adder-subtractor circuit has the following values for input mode M and data inputs A and B. In each case, determine the values of the outputs: S3, S2, S1, S0 and C4.

	M	A	B
A	0	0111	0110
B	0	1000	1001
C	1	0101	1010
D	1	0000	0001

2. Design a 4-bit combinational circuit decrementer using four full-adder circuits.

3. Design an Arithmetic circuit with one variable S and two n bit data inputs A and B. The circuits generate the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages

S	C_{in} =0	C_{in} =1
0	$D = A + B$	$D = A + 1$
1	$D = A - 1$	$D = A + \bar{B} + 1$

4. Design a digital circuit that performs the four logic operations of exclusive-OR, exclusive-NOR, NOR and NAND. Use two selection variables. Show the logic diagram of one typical stage.

5. Register A holds the 8-bit binary **11011001**. Determine the B operand and the logic micro-operation to be performed in order to change the value in A to

a. **01101101**
b. **11111101**

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In Pursuit of Excellence	**Tutorial-5**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Sr. No.	No. of Periods	Topics/Sub Topics	Coverage Date						Sign
			Section A			Section B			
			A1	A2	A3	C1	C2	C3	
1.	1	Stack Organization, Look ahead carries adder	28/09/2019	03/09/2019	18/09/2019	06/09/2019	19/09/2019	19/09/2019	

CO2

1. Convert the following arithmetic expressions from infix to reverse Polish notation:
   a) A + B * [C * D + E * (F + G)]
   b) $\frac{A*[B+C*(D+E)]}{F*(G+H)}$
2. Convert the arithmetic expression A B C D E F G + * + * + * from reverse Polish notation to infix notation.
3. Explain about Look ahead carries adder.

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In Pursuit of Excellence	**Tutorial-6**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Sr. No.	No. of Periods	Topics/Sub Topics	Coverage Date						Sign
			Section A			Section B			
			A1	A2	A3	C1	C2	C3	
1.	1	Addition and Subtraction using Signed Magnitude and 2's Complement Number, Signed Multiplication	05/09/2019	17/09/19	25/09/2019	20/09/2019	26/09/2019	26/09/2019	

CO2

1. Compute the following signed magnitude numbers and give the value of AVF. the leftmost bit in the following numbers represent the signed bit.
   a. 0 101101 + 0 011111
   b. 1 011111 + 1 101101
   c. 0 101101 – 0 011111
   d. 0 101101 – 0 101101
   e. 1 011111 – 0 101101
2. Perform the arithmetic operations on the below binary numbers and with negative numbers in signed 2's complement representation. Use seven bits to accommodate each number together with its sign. In each case, determine if there is an overflow by checking the carries into and out of the sign bit position.
   a. (+35) + (+40)
   b. (-35) + (-40)
   c. (-35) + (+40)
3. Consider the two 8-bit numbers A=01000001 and B= 10000100.
   a) Give the decimal equivalent of each number assuming that (1) they are unsigned and (2) they are signed.
   b) Add the two binary numbers and interpret the sum assuming that the numbers are (1) unsigned and (2) signed.
   c) Determine the values of C, Z, S and V status bits after the addition.
4. Perform step by step multiplication of two numbers using Signed Magnitude data.
   a. (+15) * (-13) b. (-12) * (-18) c. (+13) * (-15)

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In Pursuit of Excellence	**Tutorial-7**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Sr. No.	No. of Periods	Topics/Sub Topics	Coverage Date						Sign
			Section A			Section B			
			A1	A2	A3	C1	C2	C3	
1.	1	Booth Multiplication, Division, Multiplier, Floating Point Number	12/10/2019	01/11/2019	09/11/2019	27/09/2019	03/10/2019	03/10/2019	

CO2

1. Perform step by step multiplication of two numbers using Booth algorithm. Assume that 5-bit register hold signed number.
   b. (+15) * (-13)
   c. (-12) * (-18)
   d. (+13) * (-15)
2. Perform the division of the following positive number 1000 by 11 using 4-bit register.
3. Design an array multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders.
4. What will be the decimal value of 0.5 in IEEE single precision floating point representation?
5. Using single precision 32-bit floating point format IEEE-754 standard that uses 1 bit for sign, 8bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of -14.25. What will be the representation of X in hexadecimal notation?

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In Pursuit of Excellence	**Tutorial-8**	SESSION-2019-2020 SEM- 3rd

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Sr. No.	No. of Periods	Topics/Sub Topics	Coverage Date						Sign
			Section A			Section B			
			A1	A2	A3	C1	C2	C3	
1.	1	Instruction Format, Addressing Modes	19-10-2019	15/10/2019	16/10/2019	09/10/2019	10/10/2019	10/10/2019	

CO2

1. Evaluate the arithmetic statement X = (A+B)*(C+D) using a general register computer with three address, two address and one address instruction format a program to evaluate the expression .
2. A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.
   (i) How many bits are there in the operation code, the register code part and the address part?
   (ii) Draw the instruction word format and indicate the number of bits in each part.
   (iii) How many bits are there in the data and address inputs of the memory?

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In Pursuit of Excellence	**Tutorial-9**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Sr. No.	No. of Periods	Topics/Sub Topics	Coverage Date						Sign
			Section A			Section B			
			A1	A2	A3	C1	C2	C3	
1.	1	Memories	02/11/2019	05/11/2019	06/11/2019	11/10/2019	31/10/2019	17/10/2019	

CO4

1. Explain memory hierarchy with diagram.
2. A two way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from memory. The main memory size is 128K X 32.
   i. Formulate all pertinent information required to construct the cache memory.
   ii. What is the size of cache memory?
3. An address space is specified by the 24 bits and the corresponding memory space is by 16 bits.
   i. how many words are there in the address space
   ii. how many words are there in the memory space
   iii. If the page consists of 2k words how many pages and blocks are there in the system.
4. Discuss the various types of address mapping used in cache memory.

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In Pursuit of Excellence	**Tutorial-10**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Sr. No.	No. of Periods	Topics/Sub Topics	Coverage Date						Sign
			Section A			Section B			
			A1	A2	A3	C1	C2	C3	
1.	1	Input Output Organization	16/11/2019	19/11/2019	23/11/2019	04/11/2019	07/11/2019	31/10/2019	

CO5

1. What is peripheral device? Give the example of peripheral devices.
2. What is asynchronous data transfer? Explain.
3. Explain DMA.

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In Pursuit of Excellence	**ASSIGNMENT - 1**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

[CO- 1]

1. Convert the followings
   $(100100)_2 = (?)_{10}$
   $(235.41)_7 = (?)_{13}$
2. Perform the following operation on signed numbers using 2's compliment method:
   $(56)_{10} + (-27)_{10}$
3. Show the bit configuration of 24 bit register when its contents represent the decimal equivalent of 195 in BCD.
4. Discuss self-complementing BCD code. Represent decimal number 6,248 in:
   a. BCD
   b. Excess-3 code
   c. 2421 code
5. What is the radix of the numbers if the solution to the quadratic equation $x^2 - 10x + 31 = 0$ is $x = 5$ and $x = 8$?
6. What is multiplexer? Give some applications of multiplexer.

   Or

   Draw the circuit diagram of D Flip-Flop.
7. Explain: Serial Bus Arbitration or Parallel Bus Arbitration.
8. Define Bus system? Explain the architecture of Bus system.
9. What is asynchronous data transfer? Explain
10. Explain the interconnections between processor and memory.

    Or

    Write the function of Registers: (i) PC (ii) IR (iii) MAR (iv) MDR
11. Draw a diagram for Bus System with Multiplexers or Using Tri-state Buffers.
12. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.
    a. How many selection inputs are there in each multiplexer?
    b. What size of multiplexers are needed?
    c. How many multiplexers are there in the bus?
13. What are different micro - operations? Write their names also.
14. Represent the following conditional control statement by two register transfer statements with control functions
    If (P = 1) then (R1 ← R2) else if (Q = 1) then R1 ← R3)
15. Consider the following register transfer statements for two 4-bit registers R1 and R2.
    xT: R1← R1 + R2
    x'T : R1 ← R2
    Draw a diagram showing hardware implementation of two statements.
16. Draw a block diagram showing the hardware implementation of the register transfers
    T0: R5 ← R0
    T1: R5 ← R1
    T2: R5 ← R2
    T3: R5 ← R3
    The required transfers are dictated by four mutual exclusive timing variable T0 to T3.

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17. Design an Arithmetic circuit with one variable S and two n bit data inputs A and B. The circuits generate the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages

S	C_{in} =0	C_{in} =1
0	$D = A + B$	$D = A + 1$
1	$D = A - 1$	$D = A + \bar{B} + 1$

18. Design a digital circuit that performs the four logic operations of exclusive-OR, exclusive-NOR, NOR and NAND. Use two selection variables. Show the logic diagram of one typical stage.
19. Register A holds the 8-bit binary **11011001**. Determine the B operand and the logic micro-operation to be performed in order to change the value in A to
    c. **01101101**
    d. **11111101**
20. Give the hardware implementation of following operations;-
    a. Selective set
    b. Selective complement
21. Starting from an initial value of R = **11011101**, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical shift right and circular shift-left.
22. What is general register organization?
23. Specify the Control word that must be applied to the processor to implement the following micro-operation
    a. $R1 \leftarrow R2+R3$
    b. $R4 \leftarrow R4$
    c. $R5 \leftarrow R5 - 1$
    d. $R6 \leftarrow shl\ R1$
    e. $R7 \leftarrow input$
24. What is stack organization? Compare register stack and memory stack.
25. Let SP =**000000** in the stack. How many items are there in the stack if:
    a. FULL = 1 and EMPTY = 0
    b. FULL = 0 and EMPTY = 1
26. Convert the following arithmetic expressions from infix to reverse polish notation.
    a. $A * B + C * D + E * F$
    b. $A + B * [C * D + E * (F + G)]$
    c. $\frac{A*[B+C*(D+E)]}{F*(G+H)}$
27. Convert the following arithmetic expressions from reverse Polish notation to infix notation.
    a. $ABCDE +* -/$
    b. $ABC */D - EF/+$
28. Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operations for evaluating the numerical result.

$$(3 + 4)[10(2 + 6) + 8]$$

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In Pursuit of Excellence	ASSIGNMENT - 2	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

[CO- 2]

1. Describe carry-look ahead adder with block diagram.
2. Add -35 and -31 in binary using 8 bit registers in signed 1's complement and signed 2's complement.
3. Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation.
4. Explain Booths multiplication algorithm in detail.
5. Discuss the Booth's algorithm for twos-complement number. Also illustrate it with some example.
6. Draw the flow chart of Booth's Algorithm for multiplication and show the multiplication process using Booth's Algorithm for (-7) X (+3).
7. Show the step by step multiplication process of (15) * (-13) using Booth's Algorithm.
8. Draw the hardware details for the Booth's Multiplication algorithm and using Booth's multiplication multiply decimal numbers (-23) and (+9).
9. Show step by step the multiplication process using booth's algorithm when (+15) and (-13) numbers are multiplied. Assume 5-bit registers that holds signed numbers.
10. What is an array multiplier? Design an array multiplier that multiplies two 4-bit binary numbers. Use AND gates and Binary Adders.
11. Perform the division process of 00001111 by 0011(use a dividend of 8 bits).
12. Describe the basic format used to represent the floating-point numbers. Also define the concept of normalization and biasing with some example.
13. Explain IEEE standard for floating point representation.
14. How floating point numbers are represented in computer, also give IEEE 754 standard 32-bit floating point number format
15. Represent (-307.1875)10 in single precision and double precision format.

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In Pursuit of Excellence	**ASSIGNMENT - 3**	SESSION-2019-2020 SEM- 3rd

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[CO- 3]

1. Evaluate the arithmetic statement X = (A+B)*(C+D) using a general register computer with three address, two address and one address instruction format a program to evaluate the expression .
2. Write a program to evaluate arithmetic expression X= (A-B) * (((C-D * E) /F)*G)
   i. Using a general register computer with three address instructions.
   ii. Using a general register computer with two address instructions.
   iii. Using a general register computer with one address instructions.
   iv. Using a general register computer with zero address instructions.
3. Write a program to evaluate the arithmetic statement X=(A-B+C*(D*E-F))/(G+H*K)
   i. Using a general register computer with three address instructions.
   ii. Using an accumulator type computer with one address instructions.
   iii. Using a stack organized computer with zero address operation instructions.
4. Explain most common fields found in instruction formats. Also explain the three-address instruction and zero-address instruction formats with some example.
5. A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.
   (iv) How many bits are there in the operation code, the register code part and the address part?
   (v) Draw the instruction word format and indicate the number of bits in each part.
   (vi) How many bits are there in the data and address inputs of the memory?
6. Explain the various addressing modes with diagram.
7. Explain the following addressing modes with an example each:
   i. Direct
   ii. Register Indirect
   iii. Implied
   iv. Immediate
   v. Indexed
   vi. Relative
   vii. Indirect
8. Describe auto increment and auto decrement addressing modes with proper example.
9. An instruction is stored at location 300 with its address fields at location 301. The address field has the value 400. A processor register RI contain the number 200.
   Evaluate the effective address if the addressing mode of the instruction is (a) Direct (b) Immediate (c) Relative (d) Register Indirect (e) Index with RI as the Index register.
10. List three types of control signals.
11. How a processor executed instructions? Define the internal functional units of a processor and how they are interconnected?
12. What is an Instruction in the context of computer organisation? Explain the purpose of various elements of an instruction with the help of sample instruction format.
13. Explain all the phases of instruction cycle.
14. Write the steps in fetching a word from memory. Differentiate between branch instruction and call subroutine instruction.

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15. Explain the basic concept of Hardwired and Software control unit with neat diagrams. What are the advantages and disadvantages in each control?
16. What is a microprogram sequencer? With block diagram, explain the working of microprogram sequencer.
17. What are the difference between Horizontal and vertical micro codes?
18. What is micro code? Explain.
19. An encoded microinstruction format is to be used. Show how a 9 bit micro operation field can be divided in to sub field to specify 46 different actions.
20. Differentiate between RISC & CISC based microprocessor.
21. Write short notes on:
    i. Pipelining
    ii. Indirect addressing.
    iii. Parallelism in microinstructions
22. Discuss write back method.

In Pursuit of Excellence	**ASSIGNMENT – 4**	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

[CO- 4]

1. What is the difference between RAM and DRAM?
2. Write the difference between RAM & ROM.
3. Explain memory hierarchy with diagram.
4. What is ROM? How does PROM differ from EEPROM?
5. What are the different auxiliary memories?
6. What is flash memory?
7. Write short note on:
   i. Organisation of 2D and 2 ½ D
   ii. Virtual Memory.
8. A) How many 128 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
   B) How many lines of address bus must be used to access 2048 bytes of memory. How many of these lines will be common to all chips.
   C) How many lines must be decoded for the chip select ? Specify the size of the decoder.
9. A 8-bit computer has 16-bit address bus, the first 15 lines of the address are used to select a bank of 32k bytes of memory, the higher order bit of the address is used to select a register which receives the contents of the data bus. Explain how this configuration can be used to extend the memory capacity of the system to eight banks of 32K bytes each, for a total of 256K bytes of memory.
10. A computer employs RAM chips of 256 × 8 and ROM chips of 1024 × 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for interface registers.
    i. How many RAM and ROM chips are needed?
    ii. Draw a memory-address map for the system.
    iii. Give the address ranges in hex for RAM, ROM and interface.
11. What is the transfer rate of an 8 track magnetic tape whose speed is 120 inches per second , whose density is 1600 bits per inch.
12. Consider a disk pack with the following specifications- 16 surfaces, 128 tracks per surface, 256 sectors per track and 512 bytes per sector.
    i. What is the capacity of disk pack?
    ii. What is the number of bits required to address the sector?
    iii. If the disk is rotating at 3600 RPM, what is the data transfer rate?
    iv. If the disk system has rotational speed of 3000 RPM, what is the average access time with a seek time of 11.5 msec?
13. What is the average access time for transferring 512 bytes of data with the following specifications-
    Average seek time = 5 msec
    Disk rotation = 6000 RPM
    Data rate = 40 KB/sec
    Controller overhead = 0.1 msec
14. A moving arm disc storage device has the following specifications:
    Number of Tracks per recording surface: 200
    Disc rotation speed: 2400 revolution/minute
    Track-storage capacity: 62500 bits

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Estimate the average latency and data transfer rate of this device.

15. What is role of cache memory? Explain different cache mapping schemes.
16. Discuss the various types of address mapping used in cache memory.
17. What is associative memory? Explain with the help of a block diagram. Also mention the situation in which associative memory can be effective utilized.
18. A two way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from memory. The main memory size is 128K X 32.
    iii. Formulate all pertinent information required to construct the cache memory.
    iv. What is the size of cache memory?
19. A digital computer has a memory unit of 64K X 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.
    i. How many bits are there in the tag, index, block, and words fields of the address format?
    ii. How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.
    iii. How many blocks can cache accommodate?
20. Consider a cache uses a direct mapping scheme. The size of main memory is 4K byte and word size of a cache is 2 bytes. The size of cache memory is 128 bytes.
    Find the following:
    i. The size of main memory address (assume each byte of main memory has an address).
    ii. Address of a cache block.
    iii. How many memory location address will be translated to cache address/block/location?
    iv. How can it be determined if the content of specified memory address exists in cache.
21. What do you mean by cache memory? How does it affect the performance of the computer system? An eight-way set-associative cache is used in a computer in which the real memory size is 2^{32} bytes. The line size is 16 bytes, and there are 2^{10} lines per set. Calculate the cache size and tag length. (lines = blocks)
22. An address space is specified by the 24 bits and the corresponding memory space is by 16 bits.
23. how many words are there in the address space
24. how many words are there in the memory space
25. If the page consists of 2k words how many pages and blocks are there in the system.
26. A virtual memory has page size of 1 K words. There are 8 pages and 4 blocks. The associative memory page table contains the following entries

Page	Block
0	3
1	1
4	2
6	0

Make a list of all virtual addresses (in decimal) that will cause a page fault if used by the CPU.

In Pursuit of Excellence	**ASSIGNMENT – 5**	SESSION-2019-2020 SEM- 3rd

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[CO- 5]

IO

1. What is peripheral device? Give the example of peripheral devices.
2. What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each?

Asynchronous Data Transfer

3. What is asynchronous data transfer? Explain.
4. What do you mean by asynchronous data transfer? Explain strobe controller and hand shaking mechanism for asynchronous data transfer.
5. What is meant by synchronous and asynchronous communication?

Mode of Data transfer

6. Describe in detail about programmed Input/output with neat diagram.
7. Write short note on Interrupt.
8. Differentiate between vectored interrupt and nonvectored Interrupt.
9. Describe cycle stealing in DMA.
10. Write short notes on: DMA based data transfer.
11. Give the block diagram of DMA controller. Why are the read and write control lines in a DMA controller bidirectional?
12. Explain the working of DMA controller with help of suitable diagrams.
13. Why DMA is required? Explain its functions with the help of block diagram.

IOP

14. Write short note on Input Output Processor.
15. Discuss the working principle of I/O processor. Serial and Parallel Transfer
16. Write short note on Serial communication.
17. Write the difference between serial & parallel communication.

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In Pursuit of Excellence	List of Students	SESSION-2019-2020 SEM- 3rd

Section A

S.No	Student No	Roll No	Name of Students	Father's Name
1.	1810018	1808210001	AASHISH PAL	SARVESH KUMAR
2.	1810080	1808210002	ABHAY VARSHNEY	VIPIN KUMAR VARSHNEY
3.	1810250	1808210003	ABHAY PRATAP SINGH	DEVENDRA SINGH
4.	1810086	1808210005	ABHISHEK	DHARAMVEER SINGH
5.	1810009	1808210006	ABHISHEK KUMAR	PREM KUMAR
6.	1810083	1808210007	ABHISHEK SHARMA	DINESH CHANDRA SHARMA
7.	1810177	1808210009	ACHAL GUPTA	RAJEEV KUMAR GUPTA
8.	1810147	1808210010	ADARSH UPADHYAY	GYAN PRAKASH UPADHYAY
9.	1810253	1808210011	AHAD NUSRAT	NUSRAT HUSSAIN
10.	1810051	1808210012	AJENDAR	RAMPHOOL SINGH
11.	1810110	1808210013	AKASH BHATNAGAR	PRADEEP KUMAR BHATNAGAR
12.	1810249	1808210014	AKASH JAUHARI	DHARMENDRA KUMAR JAUHARI
13.	1810107	1808210015	AKASH KUMAR	NARESH KUMAR
14.	1810116	1808210016	AKHIL KUMAR	DEVENDRA KUMAR
15.	1810077	1808210017	AKSHITA VERMA	SANJAY KUMAR VERMA
16.	1810271	1808210018	AMAN KUMAR	GURDEEP PAL ARORA
17.	1810146	1808210019	AMAN VAISH	SANJEEV VAISH
18.	1810268	1808210020	AMBIKA MALHOTRA	ARVIND MOHAN MAHOTRA
19.	1810034	1808210021	AMIR	SHAKHAWAT HUSAIN
20.	1810194	1808210022	AMOL JAIN	NIRMAL JAIN
21.	1810078	1808210024	ANANT BANSAL	ANUP BANSAL
22.	1810071	1808210025	ANIKET SINGH	SHIV CHARAN SINGH
23.	1810235	1808210026	ANIL KUMAR	SHIVCHARAN SINGH
24.	1810202	1808210027	ANIL KUMAR	SITA RAM
25.	1810278	1808210028	ANKIT CHANDRA	MUKESH CHANDRA
26.	1810211	1808210029	ANKIT KUMAR	BHOOP SINGH
27.	1810056	1808210030	ANKUSH TYAGI	PRAVESH KUMAR TYAGI
28.	181013	1808210031	ANSHDEEP TYAGI	LATE NEERAJ TYAGI
29.	1810052	1808210032	ANSHIKA GOEL	MANOJ GOEL
30.	1810160	1808210033	ANUBHAV MISHRA	RAJESH MISHRA
31.	1810120	1808210034	ANUBHAV SHUKLA	SANJEEV SHUKLA
32.	1810138	1808210036	ASEEM GUPTA	RAKESH KUMAR GUPTA
33.	1810148	1808210037	AVNISH KUMAR	SUNIL KUMAR

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34.	1810069	1808210038	AYUSH KUMAR SINGH	UDAI BHAN SINGH
35.	1810103	1808210039	AYUSH SHARMA	RAJ KUMAR SHARMA
36.	1810241	1808210040	BHASKAR SAINI	PREM PRAKASH SAINI
37.	1810050	1808210041	BHUVNESH KUMAR SHARMA	KRISHAN AVTAR SHARMA
38.	1810022	1808210042	BILAL SAIFI	ANWAR SAIFI
39.	1810079	1808210043	BOBI KHAN	IKRAM KHAN
40.	1810179	1808210044	CHANDR VEER SINGH	VISHVA VIJAY SINGH
41.	1810135	1808210046	DEEKSHA SINGH	MAHENDRA SINGH
42.	1810277	1808210047	DEEPENDRA SINGH RAGHAV	NARENDRA SINGH RAGHAV
43.	1810234	1808210048	DEVAL JHINGRAN	RAJIV JHINGRAN
44.	1810106	1808210050	DEVESH BHARDWAJ	PAWAN BHARDWAJ
45.	1810229	1808210051	GAGAN	MAHENDRA PAL
46.	1810191	1808210052	GARVIT BHOLA	ARUN BHOLA
47.	1810011	1808210053	GAURANG GUPTA	MUKESH KUMAR GUPTA
48.	1810091	1808210054	GAURANGEE BHARDWAJ	MANISH BHARDWAJ
49.	1810109	1808210055	GAURAV BHATNAGAR	PRADEEP KUMAR BHATNAGAR
50.	1810217	1808210056	GAURAV KUMAR	RAJ PAL SINGH
51.	1810059	1808210057	GEETIKA GUPTA	KULDEEP KUMAR GUPTA
52.	1810201	1808210058	HAMMAD HUSSAIN	SAYED ZAKIR HUSSAIN
53.	1810254	1808210059	HARSH GUPTA	SURENDRA GUPTA
54.	1810270	1808210060	HARSH VARDHAN	VINEET KUMAR
55.	1810089	1808210061	HARSHBEER SINGH	PRABHJOT SINGH
56.	1810226	1808210062	HARSHIT KUMAR	SUBODH KUMAR
57.	1810181	1808210063	HARSHIT PANDEY	ANIL KUMAR PANDEY
58.	1810023	1808210064	HONEY TYAGI	MUKESH TYAGI
59.	1810144	1808210066	IRAM RAFI	MOHD RAFI
60.	1810188	1808210067	ISHAN SAXENA	SANJAY SAXENA

Batch – A1	1 – 20
Batch – A2	21-40
Batch – A3	41-REST

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Section C

S.No	Student No	Roll No	Name of Students	Father's Name
1.	1810032	1808210131	SANKALP GUPTA	RAJESH KUMAR GUPTA
2.	1810125	1808210132	SANSKRITI AGARWAL	KAPIL AGARWAL
3.	1810184	1808210133	SARTHAK SAXENA	SHASHI KANT SAXENA
4.	1810149	1808210134	SATAKSHI	MADAN MOHAN
5.	1810151	1808210135	SAURABH KUMAR	RAJ PAL SINGH
6.	1810153	1808210136	SAYYDUL MILLAT	HASNAIN AKHTER
7.	1810043	1808210137	SHAZAR ZAIDI	BADAR ZAIDI
8.	1810261	1808210138	SHIVANI TYAGI	MANGU TYAGI
9.	1810113	1808210139	SHIVANSH MATHUR	MUKUL MATHUR
10.	1810098	1808210140	SHIVANSH AGARWAL	ANIMESH AGARWAL
11.	1810257	1808210141	SHIVANSHU AGARWAL	KAMAL KUMAR
12.	1810124	1808210142	SHREY RUHELA	PRADEEP RUHELA
13.	1810042	1808210143	SHREYA CHAUHAN	SANJAY CHAUHAN
14.	1810040	1808210144	SHUBH BHATNAGAR	MANOJ BHATNAGAR
15.	1810180	1808210146	SHUBHAM YADAV	NARESH SINGH
16.	1810005	1808210147	SHUBHIKA SINGH	SANJEEV SINGH
17.	1810015	1808210148	SOURABH SAINI	UDAY RAJ SINGH
18.	1810165	1808210149	SPARSH RASTOGI	MANOJ RASTOGI
19.	1810094	1808210150	SRIJAN PANDEY	NIKUNJ PANDEY
20.	1810205	1808210151	SUFIYA	MOHD SHAKEEL
21.	1810222	1808210152	SUHAIL AHMED	MEHMOOD HASAN
22.	1810057	1808210153	SUKRITI SINGH	RAJESH SINGH
23.	1810085	1808210154	SUMIT KUMAR	SURAJ SINGH
24.	1810025	1808210155	SUSHANT KUMAR	VIJENDRA SINGH
25.	1810100	1808210156	SUSHANT SINGH	GIRVAR SINGH
26.	1810143	1808210157	TANVEER ALAM	ASHRAF ALI
27.	1810275	1808210158	UDIT RAJPUT	SATENDRA KUMAR
28.	1810001	1808210159	UMANG MATHUR	GOPAL SARAN MATHUR
29.	1810161	1808210160	UNNATI GANGWAR	GOPAL GANGWAR
30.	1810087	1808210161	UNNATI SINGH	UDAY KUMAR SINGH
31.	1810095	1808210162	UTKARSH GUPTA	SANJEEV GUPTA
32.	1810014	1808210164	VASU GOEL	HARISH KUMAR
33.	1810156	1808210165	VASUNDHRA GUPTA	AKASH GUPTA
34.	1810067	1808210166	VEDIKA AGARWAL	NAVENDU AGARWAL
35.	1810118	1808210167	VINAYAK VARSHNEY	SATISH CHANDRA GUPTA
36.	1810108	1808210168	VIRENDRA MOHAN	VINOD KUMAR
37.	1810174	1808210170	VISHAL TYAGI	DEEPAK KUMAR TYAGI

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38.	1810048	1808210171	YASH AGARWAL	GOPAL AGARWAL
39.	1810169	1808210172	ZAMAN ABBAS	AFZAL HUSAIN

Diploma

1.	2191005	1900820109001	ANUJ SHARMA	VINOD KUMAR SHARMA
2.		1900820109002	HADIYA KHALEEQ	
3.	2191009	1900820109003	SATYAM RASTOGI	SUNIL KUMAR RASTOGI
4.	2191006	1900820109004	UDIT	GIRISH CHANDRA
5.	2191011	1900820109005	ZAREEN AQIQ	MOHD AQIQ
6.		1900820108001	VISHAL SAINI	

Batch – C1	1 - 15
Batch – C2	16-30
Batch – C3	31-REST

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In Pursuit of Excellence	**Record of Monthly Attendance**	SESSION-2019-2020 SEM- 3rd

Attendance Register. Dates From: 01-08-2019 to 11-09-2019

Paper Code - KCS-302

• Course: B.Tech • Year: 2nd • Section: A | Staff Name: Praveen Saini

S. No.	Name	Student Id	Roll Number	(P)	(A)	Tot.	Tot. (%age)
1	Aashish Pal	1810018	1808210001	16	2	18	88.89
2	Abhay Varshney	1810080	1808210002	17	1	18	94.44
3	Abhay Pratap Singh	1810250	1808210003	17	1	18	94.44
4	Abhishek	1810086	1808210005	14	4	18	77.78
5	Abhishek Kumar	1810009	1808210006	15	3	18	83.33
6	Abhishek Sharma	1810083	1808210007	18	-	18	100
7	Achal Gupta	1810177	1808210009	17	1	18	94.44
8	Adarsh Upadhayay	1810147	1808210010	10	8	18	55.56
9	Ahad Nusrat	1810253	1808210011	10	8	18	55.56
10	Akash Bhatnagar	1810110	1808210013	14	4	18	77.78
11	Akash Jauhari	1810249	1808210014	15	3	18	83.33
12	Akash Kumar	1810107	1808210015	18	-	18	100
13	Akhil Kumar	1810116	1808210016	14	4	18	77.78
14	Akshita Verma	1810077	1808210017	18	-	18	100
15	Aman Kumar	1810271	1808210018	12	6	18	66.67
16	Aman Vaish	1810146	1808210019	18	-	18	100
17	Ambika Malhotra	1810268	1808210020	18	-	18	100
18	Amir	1810034	1808210021	9	9	18	50
19	Amol Jain	1810194	1808210022	8	10	18	44.44
20	Aniket Singh	1810071	1808210025	14	5	19	73.68
21	Anil Kumar	1810235	1808210026	14	5	19	73.68
22	Anil Kumar	1810202	1808210027	18	1	19	94.74
23	Ankit Chandra	1810278	1808210028	17	2	19	89.47
24	Ankit Kumar	1810211	1808210029	14	5	19	73.68
25	Ankush Tyagi	1810056	1808210030	16	3	19	84.21
26	Anshdeep Tyagi	1810013	1808210031	13	6	19	68.42
27	Anshika Goel	1810052	1808210032	18	1	19	94.74
28	Anubhav Mishra	1810160	1808210033	17	2	19	89.47
29	Anubhav Shukla	1810120	1808210034	15	4	19	78.95
30	Aseem Gupta	1810138	1808210036	19	-	19	100

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31	Avnish Kumar	1810148	1808210037	13	6	19	68.42
32	Ayush Kumar Singh	1810069	1808210038	13	6	19	68.42
33	Ayush Sharma	1810103	1808210039	18	1	19	94.74
34	Bhaskar Saini	1810241	1808210040	12	7	19	63.16
35	Bhuvnesh Kumar Sharma	1810050	1808210041	18	1	19	94.74
36	Bilal Saifi	1810022	1808210042	14	5	19	73.68
37	Bobi Khan	1810079	1808210043	8	11	19	42.11
38	Chandrveer Singh	1810179	1808210044	12	7	19	63.16
39	Deeksha Singh	1810135	1808210046	14	4	18	77.78
40	Deependra Singh Raghav	1810277	1808210047	15	3	18	83.33
41	Deval Jhingran	1810234	1808210048	13	5	18	72.22
42	Devesh Bhardwaj	1810106	1808210050	17	1	18	94.44
43	Gagan	1810229	1808210051	15	3	18	83.33
44	Garvit Bhola	1810191	1808210052	15	3	18	83.33
45	Gaurang Gupta	1810011	1808210053	14	4	18	77.78
46	Gaurangee Bhardwaj	1810091	1808210054	17	1	18	94.44
47	Gaurav Bhatnagar	1810109	1808210055	13	5	18	72.22
48	Gaurav Kumar	1810217	1808210056	17	1	18	94.44
49	Geetika Gupta	1810059	1808210057	17	1	18	94.44
50	Hammad Hussain	1810201	1808210058	13	5	18	72.22
51	Harsh Gupta	1810254	1808210059	16	2	18	88.89
52	Harsh Vardhan	1810270	1808210060	15	3	18	83.33
53	Harshbeer Singh	1810089	1808210061	17	1	18	94.44
54	Harshit Kumar	1810226	1808210062	14	4	18	77.78
55	Harshit Pandey	1810181	1808210063	14	4	18	77.78
56	Honey Tyagi	1810023	1808210064	16	2	18	88.89
57	Iram Rafi	1810144	1808210066	13	5	18	72.22
58	Ishan Saxena	1810188	1808210067	18	-	18	100
			Total	864	199		81.33

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Attendance Register. Dates From: 15-09-2019 to 21-10-2019

Paper Code - KCS-302

• Course: B.Tech • Year: 2nd • Section: A | Staff Name: Praveen Saini

S. No.	Name	Student Id	Roll Number	(P)	(A)	Tot.	Tot. (%age)
1	Aashish Pal	1810018	1808210001	18	1	19	94.74
2	Abhay Varshney	1810080	1808210002	19	-	19	100
3	Abhay Pratap Singh	1810250	1808210003	19	-	19	100
4	Abhishek	1810086	1808210005	17	2	19	89.47
5	Abhishek Kumar	1810009	1808210006	14	5	19	73.68
6	Abhishek Sharma	1810083	1808210007	18	1	19	94.74
7	Achal Gupta	1810177	1808210009	19	-	19	100
8	Adarsh Upadhayay	1810147	1808210010	13	6	19	68.42
9	Ahad Nusrat	1810253	1808210011	14	5	19	73.68
10	Akash Bhatnagar	1810110	1808210013	17	2	19	89.47
11	Akash Jauhari	1810249	1808210014	14	5	19	73.68
12	Akash Kumar	1810107	1808210015	19	-	19	100
13	Akhil Kumar	1810116	1808210016	14	5	19	73.68
14	Akshita Verma	1810077	1808210017	17	2	19	89.47
15	Aman Kumar	1810271	1808210018	9	10	19	47.37
16	Aman Vaish	1810146	1808210019	16	3	19	84.21
17	Ambika Malhotra	1810268	1808210020	19	-	19	100
18	Amir	1810034	1808210021	12	7	19	63.16
19	Amol Jain	1810194	1808210022	15	4	19	78.95
20	Aniket Singh	1810071	1808210025	15	3	18	83.33
21	Anil Kumar	1810235	1808210026	17	1	18	94.44
22	Anil Kumar	1810202	1808210027	16	2	18	88.89
23	Ankit Chandra	1810278	1808210028	12	6	18	66.67
24	Ankit Kumar	1810211	1808210029	7	11	18	38.89
25	Ankush Tyagi	1810056	1808210030	13	5	18	72.22
26	Anshdeep Tyagi	1810013	1808210031	4	14	18	22.22
27	Anshika Goel	1810052	1808210032	15	3	18	83.33
28	Anubhav Mishra	1810160	1808210033	16	2	18	88.89
29	Anubhav Shukla	1810120	1808210034	15	3	18	83.33
30	Aseem Gupta	1810138	1808210036	16	2	18	88.89
31	Avnish Kumar	1810148	1808210037	15	3	18	83.33
32	Ayush Kumar Singh	1810069	1808210038	11	7	18	61.11
33	Ayush Sharma	1810103	1808210039	16	2	18	88.89
34	Bhaskar Saini	1810241	1808210040	10	8	18	55.56
35	Bhuvnesh Kumar Sharma	1810050	1808210041	17	1	18	94.44
36	Bilal Saifi	1810022	1808210042	14	4	18	77.78

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37	Bobi Khan	1810079	1808210043	11	7	18	61.11
38	Chandrveer Singh	1810179	1808210044	11	7	18	61.11
39	Deeksha Singh	1810135	1808210046	16	3	19	84.21
40	Deependra Singh Raghav	1810277	1808210047	15	4	19	78.95
41	Deval Jhingran	1810234	1808210048	16	3	19	84.21
42	Devesh Bhardwaj	1810106	1808210050	17	2	19	89.47
43	Gagan	1810229	1808210051	14	5	19	73.68
44	Garvit Bhola	1810191	1808210052	16	3	19	84.21
45	Gaurang Gupta	1810011	1808210053	11	8	19	57.89
46	Gaurangee Bhardwaj	1810091	1808210054	18	1	19	94.74
47	Gaurav Bhatnagar	1810109	1808210055	14	5	19	73.68
48	Gaurav Kumar	1810217	1808210056	13	6	19	68.42
49	Geetika Gupta	1810059	1808210057	18	1	19	94.74
50	Hammad Hussain	1810201	1808210058	16	3	19	84.21
51	Harsh Gupta	1810254	1808210059	17	2	19	89.47
52	Harsh Vardhan	1810270	1808210060	13	6	19	68.42
53	Harshbeer Singh	1810089	1808210061	14	5	19	73.68
54	Harshit Kumar	1810226	1808210062	11	8	19	57.89
55	Harshit Pandey	1810181	1808210063	16	3	19	84.21
56	Honey Tyagi	1810023	1808210064	15	4	19	78.95
57	Iram Rafi	1810144	1808210066	15	4	19	78.95
58	Ishan Saxena	1810188	1808210067	15	4	19	78.95
			Total	854	229		78.76

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Attendance Register. Dates From: 25-10-2019 to 27-11-2019

Paper Code - KCS-302

• Course: B.Tech • Year: 2nd • Section: A | Staff Name: Praveen Saini

S. No.	Name	Student Id	Roll Number	(P)	(A)	Tot.	Tot. (%age)
1	Aashish Pal	1810018	1808210001	14	1	15	93.33
2	Abhay Varshney	1810080	1808210002	13	2	15	86.67
3	Abhay Pratap Singh	1810250	1808210003	11	4	15	73.33
4	Abhishek	1810086	1808210005	14	1	15	93.33
5	Abhishek Kumar	1810009	1808210006	7	8	15	46.67
6	Abhishek Sharma	1810083	1808210007	13	2	15	86.67
7	Achal Gupta	1810177	1808210009	14	1	15	93.33
8	Adarsh Upadhayay	1810147	1808210010	9	6	15	60
9	Ahad Nusrat	1810253	1808210011	5	10	15	33.33
10	Akash Bhatnagar	1810110	1808210013	10	5	15	66.67
11	Akash Jauhari	1810249	1808210014	15	-	15	100
12	Akash Kumar	1810107	1808210015	13	2	15	86.67
13	Akhil Kumar	1810116	1808210016	12	3	15	80
14	Akshita Verma	1810077	1808210017	15	-	15	100
15	Aman Kumar	1810271	1808210018	9	6	15	60
16	Aman Vaish	1810146	1808210019	14	1	15	93.33
17	Ambika Malhotra	1810268	1808210020	15	-	15	100
18	Amir	1810034	1808210021	13	2	15	86.67
19	Amol Jain	1810194	1808210022	7	8	15	46.67
20	Aniket Singh	1810071	1808210025	12	2	14	85.71
21	Anil Kumar	1810235	1808210026	9	5	14	64.29
22	Anil Kumar	1810202	1808210027	12	2	14	85.71
23	Ankit Chandra	1810278	1808210028	8	6	14	57.14
24	Ankit Kumar	1810211	1808210029	3	11	14	21.43
25	Ankush Tyagi	1810056	1808210030	12	2	14	85.71
26	Anshdeep Tyagi	1810013	1808210031	9	5	14	64.29
27	Anshika Goel	1810052	1808210032	12	2	14	85.71
28	Anubhav Mishra	1810160	1808210033	11	3	14	78.57
29	Anubhav Shukla	1810120	1808210034	7	7	14	50
30	Aseem Gupta	1810138	1808210036	13	1	14	92.86
31	Avnish Kumar	1810148	1808210037	6	8	14	42.86
32	Ayush Kumar Singh	1810069	1808210038	7	7	14	50
33	Ayush Sharma	1810103	1808210039	11	3	14	78.57
34	Bhaskar Saini	1810241	1808210040	3	11	14	21.43
35	Bhuvnesh Kumar Sharma	1810050	1808210041	13	1	14	92.86
36	Bilal Saifi	1810022	1808210042	9	5	14	64.29
37	Bobi Khan	1810079	1808210043	6	8	14	42.86
38	Chandrveer Singh	1810179	1808210044	12	2	14	85.71

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39	Deeksha Singh	1810135	1808210046	12	2	14	85.71
40	Deependra Singh Raghav	1810277	1808210047	7	7	14	50
41	Deval Jhingran	1810234	1808210048	11	3	14	78.57
42	Devesh Bhardwaj	1810106	1808210050	11	3	14	78.57
43	Gagan	1810229	1808210051	10	4	14	71.43
44	Garvit Bhola	1810191	1808210052	12	2	14	85.71
45	Gaurang Gupta	1810011	1808210053	9	5	14	64.29
46	Gaurangee Bhardwaj	1810091	1808210054	13	1	14	92.86
47	Gaurav Bhatnagar	1810109	1808210055	7	7	14	50
48	Gaurav Kumar	1810217	1808210056	7	7	14	50
49	Geetika Gupta	1810059	1808210057	13	1	14	92.86
50	Hammad Hussain	1810201	1808210058	11	3	14	78.57
51	Harsh Gupta	1810254	1808210059	11	3	14	78.57
52	Harsh Vardhan	1810270	1808210060	9	5	14	64.29
53	Harshbeer Singh	1810089	1808210061	13	1	14	92.86
54	Harshit Kumar	1810226	1808210062	8	6	14	57.14
55	Harshit Pandey	1810181	1808210063	11	3	14	78.57
56	Honey Tyagi	1810023	1808210064	10	4	14	71.43
57	Iram Rafi	1810144	1808210066	12	2	14	85.71
58	Ishan Saxena	1810188	1808210067	12	2	14	85.71
			Total	607	224		72.92

Dr. Somesh Kumar
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Attendance Register. Dates From: 01-08-2019 to 11-09-2019

Paper Code - KCS-302

• Course: B.Tech • Year: 2nd • Section: C | Staff Name: Praveen Saini

S. No.	Name	Student Id	Roll Number	(P)	(A)	Tot.	Tot. (%age)
1	Sankalp Gupta	1810032	1808210131	16	4	20	80
2	Sanskriti Agarwal	1810125	1808210132	13	7	20	65
3	Sarthak Saxena	1810184	1808210133	15	5	20	75
4	Satakshi	1810149	1808210134	15	5	20	75
5	Saurabh Kumar	1810151	1808210135	18	2	20	90
6	Sayydul Millat	1810153	1808210136	10	10	20	50
7	Shazar Zaidi	1810043	1808210137	17	3	20	85
8	Shivani Tyagi	1810261	1808210138	10	10	20	50
9	Shivansh Mathur	1810113	1808210139	13	7	20	65
10	Shivansh Agarwal	1810098	1808210140	19	1	20	95
11	Shivanshu Agarwal	1810257	1808210141	16	4	20	80
12	Shrey Ruhela	1810124	1808210142	15	5	20	75
13	Shreya Chauhan	1810042	1808210143	13	7	20	65
14	Shubh Bhatnagar	1810040	1808210144	18	2	20	90
15	Shubham Yadav	1810180	1808210146	15	5	20	75
16	Shubhika Singh	1810005	1808210147	15	3	18	83.33
17	Sourabh Saini	1810015	1808210148	14	4	18	77.78
18	Sparsh Rastogi	1810165	1808210149	14	4	18	77.78
19	Srijan Pandey	1810094	1808210150	12	6	18	66.67
20	Sufiya	1810205	1808210151	14	4	18	77.78
21	Suhail Ahmed	1810222	1808210152	7	11	18	38.89
22	Sukirti Singh	1810057	1808210153	9	9	18	50
23	Sumit Kumar	1810085	1808210154	15	3	18	83.33
24	Sushant Kumar	1810025	1808210155	15	3	18	83.33
25	Sushant Singh	1810100	1808210156	11	7	18	61.11
26	Tanveer Alam	1810143	1808210157	16	2	18	88.89
27	Udit Rajput	1810275	1808210158	15	3	18	83.33
28	Umang Mathur	1810001	1808210159	13	5	18	72.22
29	Unnati Gangwar	1810161	1808210160	13	5	18	72.22
30	Unnati Singh	1810087	1808210161	13	5	18	72.22
31	Utkarsh Gupta	1810095	1808210162	15	3	18	83.33
32	Vasu Goel	1810014	1808210164	8	10	18	44.44
33	Vasundhra Gupta	1810156	1808210165	14	4	18	77.78
34	Vedika Agarwal	1810067	1808210166	13	5	18	72.22
35	Vinayak Varshney	1810118	1808210167	18	-	18	100
36	Virendra Mohan	1810108	1808210168	14	4	18	77.78
37	Vishal Tyagi	1810174	1808210170	14	4	18	77.78
38	Yash Agarwal	1810048	1808210171	15	3	18	83.33

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39	Zaman Abbas	1810169	1808210172	8	10	18	44.44
40	Vishal Saini	2191016	1900820108001	15	3	18	83.33
41	Anuj Sharma	2191005	1900820109001	12	6	18	66.67
42	Hadiya Khaleeq	2191021	1900820109002	10	8	18	55.56
43	Satyam Rastogi	2191009	1900820109003	17	1	18	94.44
44	Udit	2191006	1900820109004	17	1	18	94.44
45	Zareen Aqiq	2191011	1900820109005	10	8	18	55.56
			Total	619	221		73.67

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Attendance Register. Dates From: 15-09-2019 to 21-10-2019

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• Course: B.Tech • Year: 2nd • Section: C | Staff Name: Praveen Saini

S. No.	Name	Student Id	Roll Number	(P)	(A)	Tot.	Tot. (%age)
1	Sankalp Gupta	1810032	1808210131	14	1	15	93.33
2	Sanskriti Agarwal	1810125	1808210132	8	7	15	53.33
3	Sarthak Saxena	1810184	1808210133	8	7	15	53.33
4	Satakshi	1810149	1808210134	6	9	15	40
5	Saurabh Kumar	1810151	1808210135	14	1	15	93.33
6	Sayydul Millat	1810153	1808210136	15	-	15	100
7	Shazar Zaidi	1810043	1808210137	14	1	15	93.33
8	Shivani Tyagi	1810261	1808210138	13	2	15	86.67
9	Shivansh Mathur	1810113	1808210139	8	7	15	53.33
10	Shivansh Agarwal	1810098	1808210140	15	-	15	100
11	Shivanshu Agarwal	1810257	1808210141	9	6	15	60
12	Shrey Ruhela	1810124	1808210142	12	3	15	80
13	Shreya Chauhan	1810042	1808210143	10	5	15	66.67
14	Shubh Bhatnagar	1810040	1808210144	10	5	15	66.67
15	Shubham Yadav	1810180	1808210146	13	2	15	86.67
16	Shubhika Singh	1810005	1808210147	10	6	16	62.5
17	Sourabh Saini	1810015	1808210148	15	1	16	93.75
18	Sparsh Rastogi	1810165	1808210149	12	4	16	75
19	Srijan Pandey	1810094	1808210150	9	7	16	56.25
20	Sufiya	1810205	1808210151	13	3	16	81.25
21	Suhail Ahmed	1810222	1808210152	16	-	16	100
22	Sukirti Singh	1810057	1808210153	14	2	16	87.5
23	Sumit Kumar	1810085	1808210154	14	2	16	87.5
24	Sushant Kumar	1810025	1808210155	14	2	16	87.5
25	Sushant Singh	1810100	1808210156	8	8	16	50
26	Tanveer Alam	1810143	1808210157	13	3	16	81.25
27	Udit Rajput	1810275	1808210158	15	1	16	93.75
28	Umang Mathur	1810001	1808210159	13	3	16	81.25
29	Unnati Gangwar	1810161	1808210160	4	12	16	25
30	Unnati Singh	1810087	1808210161	15	1	16	93.75
31	Utkarsh Gupta	1810095	1808210162	12	5	17	70.59
32	Vasu Goel	1810014	1808210164	11	6	17	64.71
33	Vasundhra Gupta	1810156	1808210165	13	4	17	76.47
34	Vedika Agarwal	1810067	1808210166	13	4	17	76.47
35	Vinayak Varshney	1810118	1808210167	17	-	17	100
36	Virendra Mohan	1810108	1808210168	12	5	17	70.59
37	Vishal Tyagi	1810174	1808210170	11	6	17	64.71

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38	Yash Agarwal	1810048	1808210171	15	2	17	88.24
39	Zaman Abbas	1810169	1808210172	17	-	17	100
40	Vishal Saini	2191016	1900820108001	10	7	17	58.82
41	Anuj Sharma	2191005	1900820109001	11	6	17	64.71
42	Hadiya Khaleeq	2191021	1900820109002	16	1	17	94.12
43	Satyam Rastogi	2191009	1900820109003	16	1	17	94.12
44	Udit	2191006	1900820109004	11	6	17	64.71
45	Zareen Aqiq	2191011	1900820109005	12	5	17	70.59
			Total	551	169		76.48

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Attendance Register. Dates From: 25-10-2019 to 27-11-2019

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• Course: B.Tech • Year: 2nd • Section: C | Staff Name: Praveen Saini

S. No.	Name	Student Id	Roll Number	(P)	(A)	Tot.	Tot. (%age)
1	Sankalp Gupta	1810032	1808210131	14	1	15	93.33
2	Sanskriti Agarwal	1810125	1808210132	9	6	15	60
3	Sarthak Saxena	1810184	1808210133	5	10	15	33.33
4	Satakshi	1810149	1808210134	7	8	15	46.67
5	Saurabh Kumar	1810151	1808210135	11	4	15	73.33
6	Sayydul Millat	1810153	1808210136	9	6	15	60
7	Shazar Zaidi	1810043	1808210137	11	4	15	73.33
8	Shivani Tyagi	1810261	1808210138	8	7	15	53.33
9	Shivansh Mathur	1810113	1808210139	8	7	15	53.33
10	Shivansh Agarwal	1810098	1808210140	10	5	15	66.67
11	Shivanshu Agarwal	1810257	1808210141	-	15	15	0
12	Shrey Ruhela	1810124	1808210142	10	5	15	66.67
13	Shreya Chauhan	1810042	1808210143	6	9	15	40
14	Shubh Bhatnagar	1810040	1808210144	7	8	15	46.67
15	Shubham Yadav	1810180	1808210146	8	7	15	53.33
16	Shubhika Singh	1810005	1808210147	8	7	15	53.33
17	Sourabh Saini	1810015	1808210148	11	4	15	73.33
18	Sparsh Rastogi	1810165	1808210149	4	11	15	26.67
19	Srijan Pandey	1810094	1808210150	5	10	15	33.33
20	Sufiya	1810205	1808210151	9	6	15	60
21	Suhail Ahmed	1810222	1808210152	11	4	15	73.33
22	Sukirti Singh	1810057	1808210153	7	8	15	46.67
23	Sumit Kumar	1810085	1808210154	9	6	15	60
24	Sushant Kumar	1810025	1808210155	9	6	15	60
25	Sushant Singh	1810100	1808210156	7	8	15	46.67
26	Tanveer Alam	1810143	1808210157	9	6	15	60
27	Udit Rajput	1810275	1808210158	12	3	15	80
28	Umang Mathur	1810001	1808210159	7	8	15	46.67
29	Unnati Gangwar	1810161	1808210160	6	9	15	40
30	Unnati Singh	1810087	1808210161	7	8	15	46.67
31	Utkarsh Gupta	1810095	1808210162	7	8	15	46.67
32	Vasu Goel	1810014	1808210164	6	9	15	40
33	Vasundhra Gupta	1810156	1808210165	9	6	15	60
34	Vedika Agarwal	1810067	1808210166	10	5	15	66.67
35	Vinayak Varshney	1810118	1808210167	14	1	15	93.33
36	Virendra Mohan	1810108	1808210168	8	7	15	53.33

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37	Vishal Tyagi	1810174	1808210170	7	8	15	46.67
38	Yash Agarwal	1810048	1808210171	12	3	15	80
39	Zaman Abbas	1810169	1808210172	6	9	15	40
40	Vishal Saini	2191016	1900820108001	6	9	15	40
41	Anuj Sharma	2191005	1900820109001	11	4	15	73.33
42	Hadiya Khaleeq	2191021	1900820109002	10	5	15	66.67
43	Satyam Rastogi	2191009	1900820109003	15	-	15	100
44	Udit	2191006	1900820109004	7	8	15	46.67
45	Zareen Aqiq	2191011	1900820109005	7	8	15	46.67
			Total	379	296		56.15

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In Pursuit of Excellence	Class Test Papers with Solution	SESSION-2019-2020 SEM- 3rd

MIT MORADABAD

B.Tech: 2nd Year,3rd Sem **Computer Organization & Architecture (KCS302)** **CT1**
Branch: CSE **Section: A,B,C** **MM: 15** **Time: 1Hr.**

All Questions are compulsory.

SECTION – A (CO-1)

1. What do you understand by Bus. Explain with its types. [1]

2. Consider the following register transfer statements for two 4-bit registers R1 and R2. Draw a diagram showing hardware implementation of two statements. [2]

$xT: R1 \leftarrow R1 + R2$
$x'T: R1 \leftarrow R2$

3. Draw a diagram that shows the interconnection between processor and Memory. [2]

4. Specify the Control word that must be applied to the processor to implement the following micro-operation [2]

1. $R1 \leftarrow R2+R3$
   $R4 \leftarrow R4$

5. Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operations for evaluating the numerical result. [2]

$$((10 * (6/((9 + 3) * 11))) + 17) + 5$$

6. How the bus system is implemented using Multiplexer and four registers A to D with 4 bits each, to transfer information from any register to any other register? Specifically, show the connections that must be included to provide a path from the outputs of register C to the inputs of register A. [3]

SECTION – B (CO-2)

7. Design an Arithmetic circuit with one variable S and two n bit data inputs A and B. The circuits generate the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages [3]

S	C_{in} =0	C_{in} =1
0	D= A+B	D= A+1
1	D = A-1	D= A+B'+1

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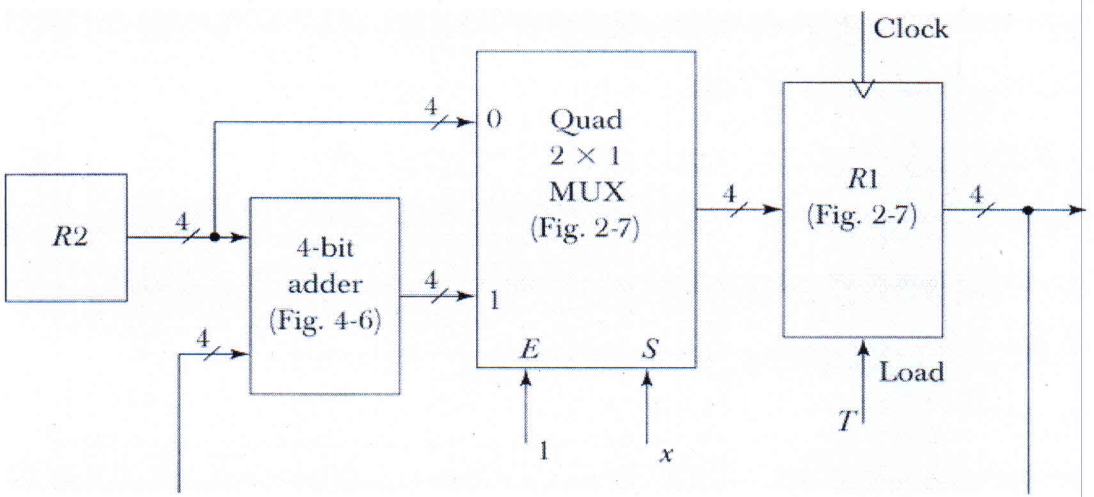
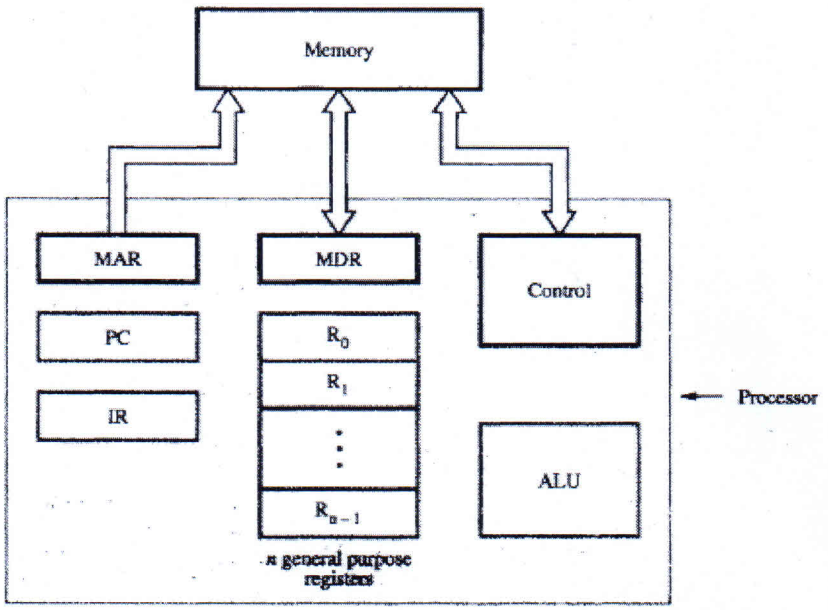
CT-1 Solution

1. **Bus** is a communication pathway connecting two or more devices. It is of three types:
   a. **Data Bus**: It provides a path for moving data between system modules.
   b. **Address Bus**: It specifies where to store the data or from where to retrieve the data.
   c. **Control Bus**: It provides a gateway for transmitting and receiving control signals between the microprocessor and various devices attached to it.

2. **Diagram shows the hardware implementation of** $xT: R1 \leftarrow R1 + R2, x'T : R1 \leftarrow R2$



3. **Below diagram shows the interconnection between processor and memory:**



4. **Control Word of following micro-operations**

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Microopeartion	SELA	SELB	SELD	OPR	Control Word
$R1 \leftarrow R2 + R3$	R2	R3	R1	ADD	010 011 001 00010
$R4 \leftarrow R4$	R4	-	R4	TSF	100 XXX 100 00000

5. Expression P: $(((10 * (6/((9 + 3) * 11))) + 17) + 5)$

Symbol Scanned	Stack	Postfix Expression
(	(	
(	((	
(	(((	
10		10
*	(((*	
(	(((*(	
6		10,6
/	(((*(/	
(	(((*(/(	
(	(((*(/((	
9		10,6,9
+	(((*(/((+	
3		10,6,9,3
)	(((*(/(	10,6,9,3,+
*	(((*(/(*	
11		10,6,9,3,+,11
)	(((*(/	10,6,9,3,+,11,*
)	(((*	10,6,9,3,+,11,*,/
)		10,6,9,3,+,11,*,/,*
+	((+	
17		10,6,9,3,+,11,*,/,*,17
)	(	10,6,9,3,+,11,*,/,*,17,+
+	(+	
5		10,6,9,3,+,11,*,/,*,17,+,5
)	-	10,6,9,3,+,11,*,/,*,17,+,5,+

Evaluation of Postfix Expression : 10,6,9,3,+,11,*,/,*,17,+,5,+

Symbol Scanned	Stack
10	**10**
6	**10,6**
9	**10,6,9**
3	**10,6,9,3**
+	**10,6,12**
11	**10,6,12,11**
*	**10,6,132**
/	**10,0**
*	**0**
17	**0,17**
+	**17**
5	**17,5**
+	**22**

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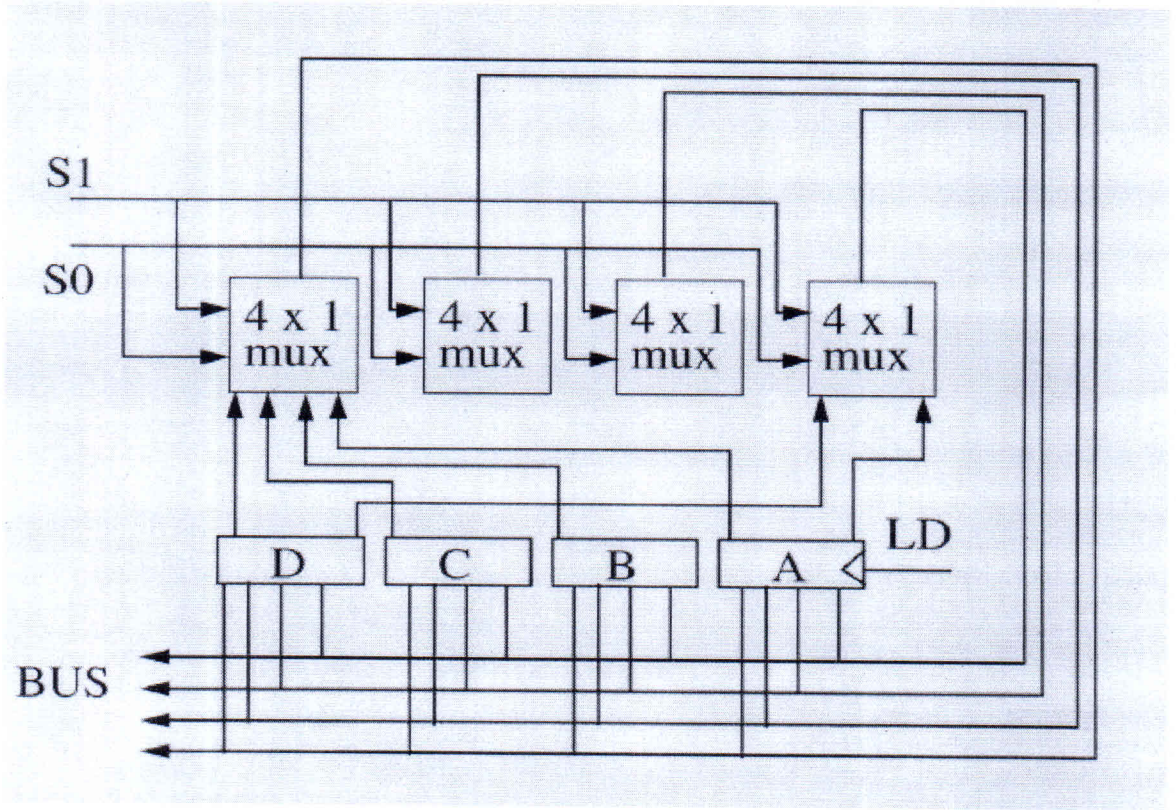
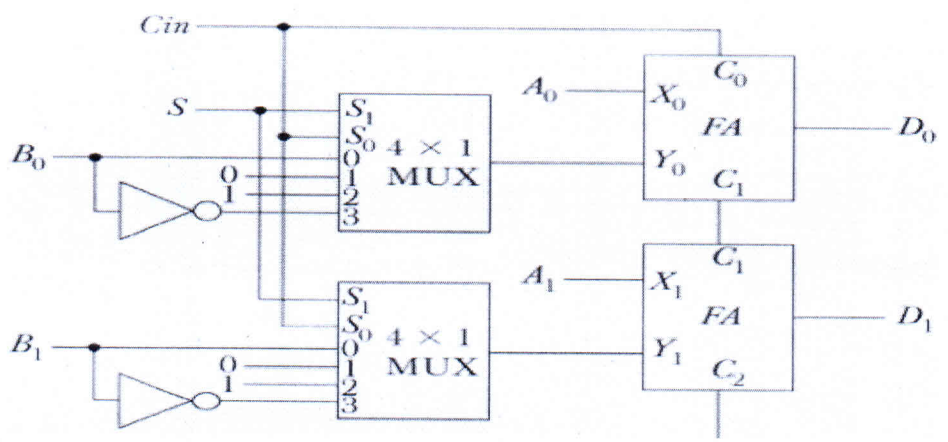
6. Implementation of Bus using Multiplexer



7.

S	Cin	X	Y	Arithmetic Operation
0	0	A	B	A+B
0	1	A	0	A+1
1	0	A	1	A-1
1	1	A	B'	A-B

Arithmetic Circuit -



Moradabad Institute of Technology
Department of CS & E
Sessional Test-2

Course: B.Tech | **Semester: 3rd**
Session: 2019-20 | **Section: A,B,C**
Sub: Computer Organization & Architecture | **Code: KCS302**
Max Marks: 15 | **Time: 1 H 15 M**

Q.No	1	2	3	4	5	6
CO	CO2	CO2	CO2	CO2	CO3	CO3

All Questions are compulsory.

SECTION – A **Marks**

1. Represent (-307.1875)10 in single precision and double precision format. **2**
2. What is an array multiplier? Design an 4 * 3 array multiplier. Use AND gates and Binary Adders. **2**
3. Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 2's complement presentation. **2**

SECTION – B

4. Show the step by step multiplication process of (+15) * (-13) using Booth's Algorithm. Assume 5-bit registers that hold signed numbers. **3**
5. Evaluate the arithmetic statement : **3**
   X = (A+B)*(C+D)
   using a general register computer with three address, two address and one address instruction format.
6. An instruction is stored at location 300 with its address field at location 301. The address field has value 400 and a processor register R1 contain a value 200. Evaluate the effective address EA if the addressing mode of the instruction is **3**
   (i) Direct (ii) Immediate (iii) Relative Addressing

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Solution of CT2

1. **Represent (-307.1875)10 in single precision and double precision format.**

$(-307.1875)_{10}$ = -100110011.0011

= -1.001100110011 * 2^{+8}

Single Precision :

Sign Bit = 1

Biased Exponent = 8 + 127 = 135 = 10000111

Mantissa = 001100110011

1	10000111	00110011001100000.....

Double Precision :

Sign Bit = 1

Biased Exponent = 8 + 1023 = 1031 = 10000000111

Mantissa = 001100110011

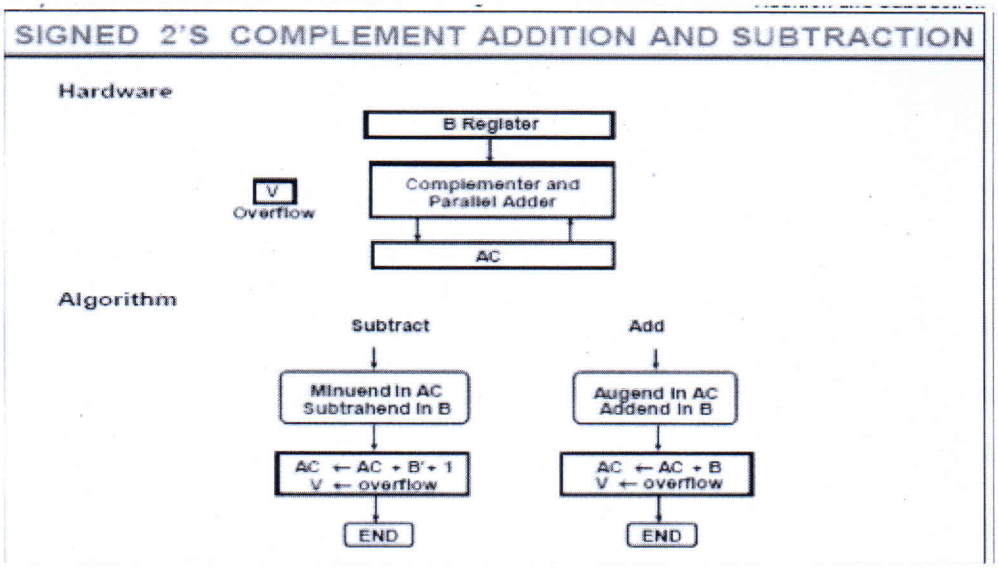
1	10000000111	00110011001100000.....

2. **What is an array multiplier? Design an 4 * 3 array multiplier. Use AND gates and Binary Adders**

Array multiplier is well known due to its regular structure. Multiplier circuit is based on add and shift algorithm. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product are shifted according to their bit orders and then added. The addition can be performed with normal carry propagate adder. N-1 adders are required where N is the multiplier length.

				A3	A2	A1	A0	Inputs
			x	B3	B2	B1	B0	
			C	B0 x A3	B0 x A2	B0 x A1	B0 x A0	
		+	B1 x A3	B1 x A2	B1 x A1	B1 x A0		
		C	sum	sum	sum	sum		
	+	B2 x A3	B2 x A2	B2 x A1	B2 x A0			Internal Signals
	C	sum	sum	sum	sum			
+	B3 x A3	B3 x A2	B3 x A1	B3 x A0				
C	sum	sum	sum	sum				
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Outputs

3. **Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 2's complement presentation.**



4. **Show the step by step multiplication process of (+15) * (-13) using Booth's Algorithm. Assume 5-bit registers that hold signed numbers.**

Refer Notes

5. **Evaluate the arithmetic statement :**

X = (A+B)*(C+D)

using a general register computer with three address, two address and one address instruction format.

Refer Notes

6. An instruction is stored at location 300 with its address field at location 301. The address field has value 400 and a processor register R1 contain a value 200. Evaluate the effective address EA if the addressing mode of the instruction is

(i) Direct (ii) Immediate (iii) Relative Addressing

Refer Notes

Moradabad Institute of Technology
Department of CS & E
Sessional Test-3

Course: B.Tech | **Semester: 3rd**
Session: 2019-20 | **Section: A,B,C**
Sub: Computer Organization & Architecture | **Code: KCS302**
Max Marks: 15 | **Time: 1 H 15 M**

Q.No	1	2	3	4	5	6
CO	CO3	CO3	CO5	CO4	CO4	CO5

All Questions are compulsory.

SECTION-A

1. Explain all the phases of instruction cycle. [2]
2. Differentiate between Hardwired & Microprogrammed Control Unit [2]
3. Explain Direct Memory Access (DMA) [2]

SECTION-B

4. Explain memory hierarchy with diagram. [3]
5. Consider a cache uses a direct mapping scheme. The size of main memory is 4K byte and word size of a cache is 2 bytes. The size of cache memory is 128 bytes. Find the following: [3]
   i. The size of main memory address (assume each byte of main memory has an address).
   ii. Address of a cache block.
   iii. How many memory location address will be translated to cache address/block/location?
6. Explain about Asynchronous Data Transfer with neat and clean diagrams. [3]

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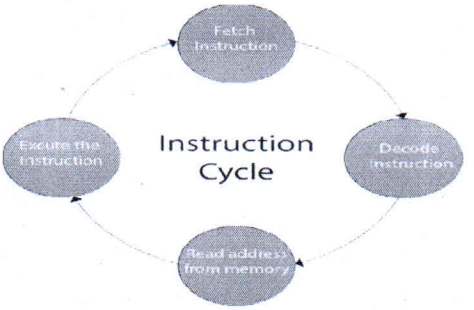
CT3 Solution

1. Explain all the phases of instruction cycle. [2]

A program residing in the memory unit of a computer consists of a sequence of instructions. These instructions are executed by the processor by going through a cycle for each instruction.

In a basic computer, each instruction cycle consists of the following phases:

1. Fetch instruction from memory.
2. Decode the instruction.
3. Read the effective address from memory.
4. Execute the instruction.



2. Differentiate between Hardwired & Microprogrammed Control Unit [2]

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A unit that uses combinational logic units, featuring a finite number of gates that can generate specific results based on the instructions that were used to invoke those responses	A unit that contains microinstructions in the control memory to produce control signals
Speed of operations is fast	Speed of operations is slow because it requires frequent memory accesses
To do modifications, the entire unit should be redesigned	Modifications can be implemented by changing the microinstructions in the control memory
More costly to implement	Less costly to implement
It is difficult to handle complex instructions	It is easier to handle complex instructions
It is difficult to perform instruction decoding	Less difficult to perform instruction decoding
Uses a small instruction set	Ues a large instruction set
There is no control memory usage	Uses control memory
Used in processors that use a simple instruction set known as the Reduced Instruction Set Computers (RISC)	Used in processors based on a complex instruction set known as Complex Instruction Set Computer (CISC)

3. Explain Direct Memory Access (DMA) [2]

The data transfer between a fast storage media such as magnetic disk and memory unit is limited by the speed of the CPU. Thus we can allow the peripherals directly communicate with each other using the memory buses, removing the intervention of the CPU. This type of data transfer technique is known as DMA or direct memory access. During DMA the CPU is idle and it has no control over the memory buses. The DMA controller takes over the buses to manage the transfer directly between the I/O devices and the memory unit.

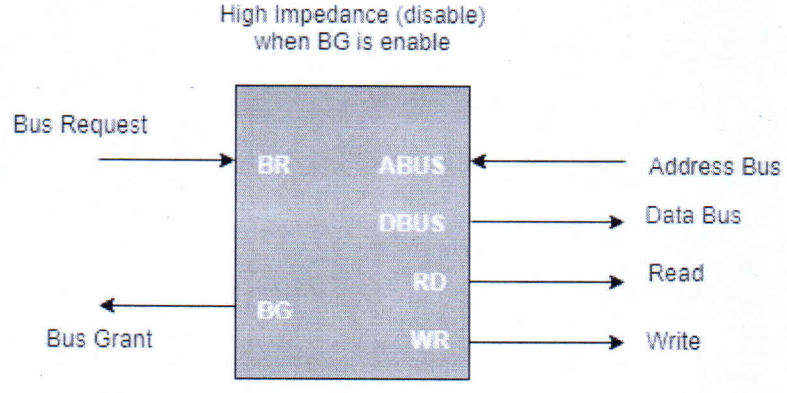


Figure - CPU Bus Signals for DMA Transfer

Bus Request : It is used by the DMA controller to request the CPU to relinquish the control of the buses.
Bus Grant : It is activated by the CPU to Inform the external DMA controller that the buses are in high impedance state and the requesting DMA can take control of the buses. Once the DMA has taken the control of the buses it transfers the data. This transfer can take place in many ways.

Types of DMA transfer using DMA controller:

Burst Transfer :

DMA returns the bus after complete data transfer. A register is used as a byte count, being decremented for each byte transfer, and upon the byte count reaching zero, the DMAC will release the bus. When the DMAC operates in burst mode, the CPU is halted for the duration of the data transfer.

Steps involved are:

a. Bus grant request time.
b. Transfer the entire block of data at transfer rate of device because the device is usually slow than the speed at which the data can be transferred to CPU.
c. Release the control of the bus back to CPU
So, total time taken to transfer the N bytes
= Bus grant request time + (N) * (memory transfer rate) + Bus release control time.

Cyclic Stealing :

An alternative method in which DMA controller transfers one word at a time after which it must return the control of the buses to the CPU. The CPU delays its operation only for one memory cycle to allow the direct memory I/O transfer to "steal" one memory cycle.

Steps Involved are:

1. Buffer the byte into the buffer
2. Inform the CPU that the device has 1 byte to transfer (i.e. bus grant request)
3. Transfer the byte (at system bus speed)
4. Release the control of the bus back to CPU.

Before moving on transfer next byte of data, device performs step 1 again so that bus isn't tied up and the transfer won't depend upon the transfer rate of device.

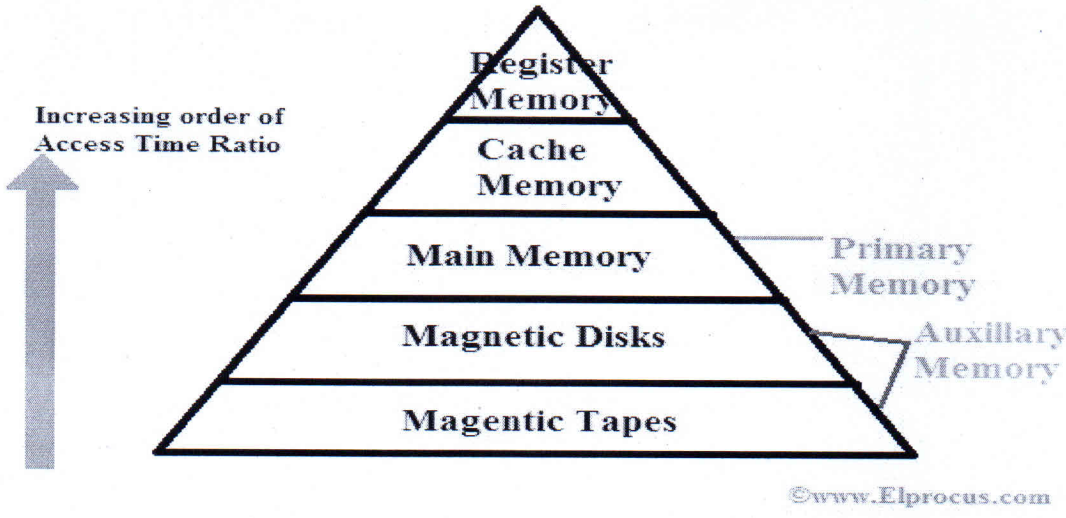
So, for 1 byte of transfer of data, time taken by using cycle stealing mode (T).
= time required for bus grant + 1 bus cycle to transfer data + time required to release the bus, it will be N x T

In cycle stealing mode we always follow pipelining concept that when one byte is getting transferred then Device is parallel preparing the next byte. "The fraction of CPU time to the data transfer time" if asked then cycle stealing mode is used.

Interleaved mode: In this technique , the DMA controller takes over the system bus when the microprocessor is not using it.An alternate half cycle i.e. half cycle DMA + half cycle processor.

4. Explain memory hierarchy with diagram. [3]

The **memory hierarchy design** in a computer system mainly includes different storage devices. Most of the computers were inbuilt with extra storage to run more powerfully beyond the main memory capacity. The following **memory hierarchy diagram** is a hierarchical pyramid for computer memory. The designing of the memory hierarchy is divided into two types such as primary (Internal) memory and secondary (External) memory.



Primary Memory

The primary memory is also known as internal memory, and this is accessible by the processor straightly. This memory includes main, cache, as well as CPU registers.

Secondary Memory

The secondary memory is also known as external memory, and this is accessible by the processor through an input/output module. This memory includes an optical disk, magnetic disk, and magnetic tape.

5. Consider a cache uses a direct mapping scheme. The size of main memory is 4K byte and word size of a cache is 2 bytes. The size of cache memory is 128 bytes. Find the following: [3]
   i. The size of main memory address (assume each byte of main memory has an address).
   ii. Address of a cache block.
   iii. How many memory location address will be translated to cache address/block/location?

MM = 4K Byte = 2^{12} * 8
CM = 128 bytes
Word size of a cache is 2 bytes, Therefore, No. of words in cache = No. of blocks in cache = 128/2 = 64

i) Size of MM Address = 12 bits
ii) Address of Cache block = 6 bits
iii) 64 memory location address will be translated to cache address/block/location

6. Explain about Asynchronous Data Transfer with neat and clean diagrams. [3]

We know that, the internal operations in individual unit of digital system are synchronized by means of clock pulse, means clock pulse is given to all registers within a unit, and all data transfer among internal registers occur simultaneously during occurrence of clock pulse. Now, suppose any two units of digital system are designed independently such as CPU and I/O interface.

And if the registers in the interface(I/O interface) share a common clock with CPU registers, then transfer between the two units is said to be synchronous. But in most cases, the internal timing in each unit is independent from each

other in such a way that each uses its own private clock for its internal registers. In that case, the two units are said to be asynchronous to each other, and if data transfer occur between them this data transfer is said to be Asynchronous Data Transfer.

But, the Asynchronous Data Transfer between two independent units requires that control signals be transmitted between the communicating units so that the time can be indicated at which they send data.

This asynchronous way of data transfer can be achieved by two methods:

1. One way is by means of strobe pulse which is supplied by one of the units to other unit. When transfer has to occur.This method is known as "Strobe Control".
2. Another method commonly used is to accompany each data item being transferred with a control signal that indicates the presence of data in the bus. The unit receiving the data item responds with another signal to acknowledge receipt of the data. This method of data transfer between two independent units is said to be "Handshaking".

The strobe pulse and handshaking method of asynchronous data transfer are not restricted to I/O transfer. In fact, they are used extensively on numerous occasion requiring transfer of data between two independent units. So, here we consider the transmitting unit as source and receiving unit as destination.

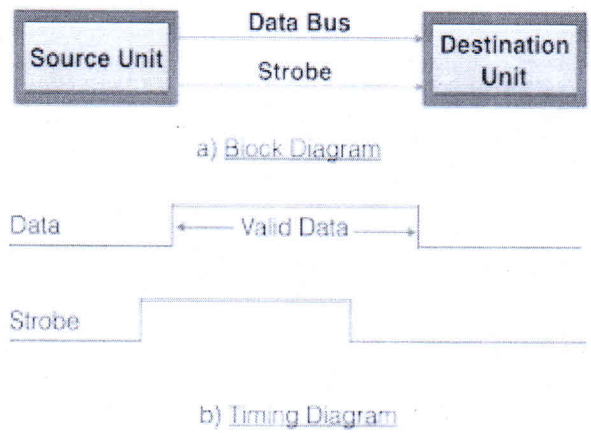
And thus, the sequence of control during an asynchronous transfer depends on whether the transfer is initiated by the source or by the destination.

So, while discussing each way of data transfer asynchronously we see the sequence of control in both terms when it is initiated by source or when it is initiated by destination. In this way, each way of data transfer, can be further divided into parts, source initiated and destination initiated.

We can also specify, asynchronous transfer between two independent units by means of a timing diagram that shows the timing relationship that exists between the control and the data buses.

1. ***Strobe Control:*** *The Strobe Control method of asynchronous data transfer employs a single control line to time each transfer .This control line is also known as strobe and it may be achieved either by source or destination, depending on which initiate transfer*

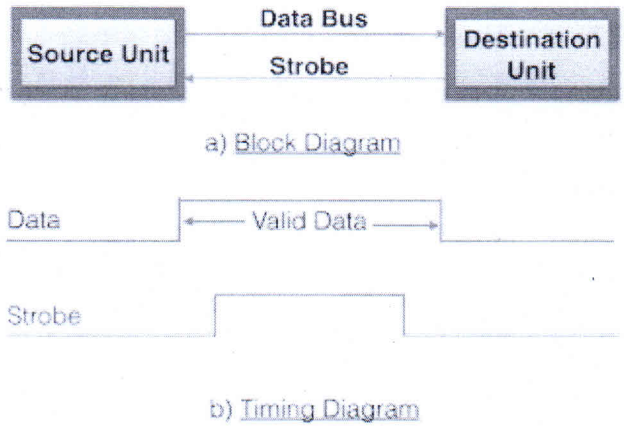
Source initiated strobe for data transfer: The block diagram and timing diagram of strobe initiated by source unit is shown in figure below:



In block diagram we see that strobe is initiated by source, and as shown in timing diagram, the source unit first places the data on the data bus. After a brief delay to ensure that the data settle to a steady value, the

source activates a strobe pulse. The information on data bus and strobe control signal remain in the active state for a sufficient period of time to allow the destination unit to receive the data. Actually, the destination unit, uses a falling edge of strobe control to transfer the contents of data bus to one of its internal registers. The source removes the data from the data bus after it disables its strobe pulse. New valid data will be available only after the strobe is enabled again.

Destination-initiated strobe for data transfer: The block diagram and timing diagram of strobe initiated by destination is shown in figure below:



In block diagram, we see that, the strobe initiated by destination, and as shown in timing diagram, the destination unit first activates the strobe pulse, informing the source to provide the data. The source unit responds by placing the requested binary information on the data bus. The data must be valid and remain in the bus long enough for the destination unit to accept it. The falling edge of strobe pulse can be used again to trigger a destination register. The destination unit then disables the strobe. And source removes the data from data bus after a per determine time interval.

Now, actually in computer, in the first case means in strobe initiated by source - the strobe may be a memory-write control signal from the CPU to a memory unit. The source, CPU, places the word on the data bus and informs the memory unit, which is the destination, that this is a write operation.

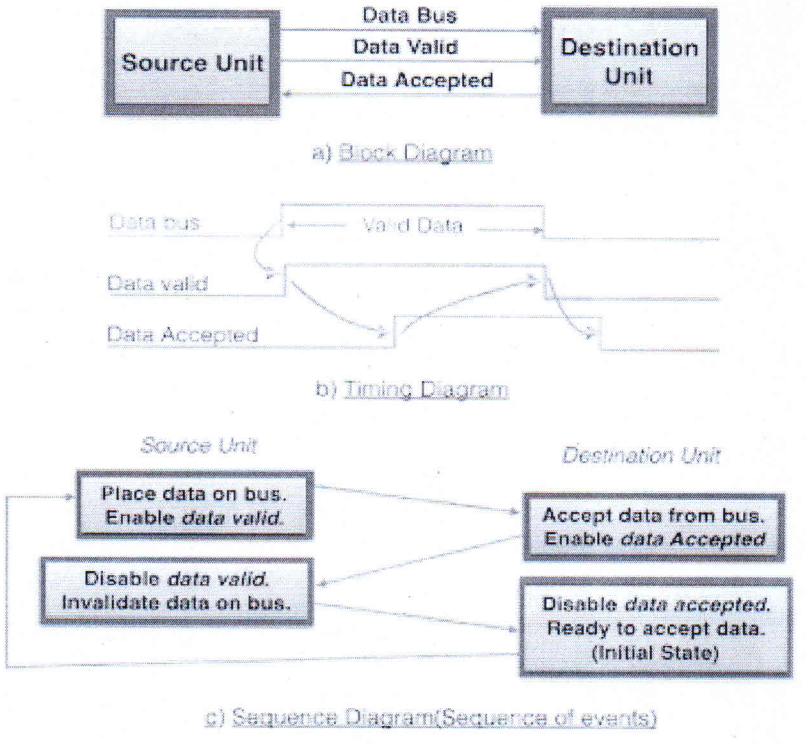
And in the second case i.e, in the strobe initiated by destination - the strobe may be a memory read control from the CPU to a memory unit. The destination, the CPU, initiates the read operation to inform the memory, which is a source unit, to place selected word into the data bus.

2. Handshaking: The disadvantage of strobe method is that source unit that initiates the transfer has no way of knowing whether the destination has actually received the data that was placed in the bus.Similarly, a destination unit that initiates the transfer has no way of knowing whether the source unit, has actually placed data on the bus. This problem can be solved by handshaking method.

Hand shaking method introduce a second control signal line that provides a replay to the unit that initiates the transfer. In it, one control line is in the same direction as the data flow in the bus from the source to destination. It is used by source unit to inform the destination unit whether there are valid data in the bus. The other control line is in the other direction from destination to the source. It is used by the destination unit to inform the source whether it can accept data. And in it also, sequence of control depends on unit that

initiate transfer. Means sequence of control depends whether transfer is initiated by source and destination. Sequence of control in both of them are described below:

Source initiated Handshaking: The source-initiated transfer using handshaking lines is shown in figure below:



In its block diagram, we see that two handshaking lines are "data valid", which is generated by the source unit, and "data accepted", generated by the destination unit.

The timing diagram shows the timing relationship of exchange of signals between the two units. Means as shown in its timing diagram, the source initiates a transfer by placing data on the bus and enabling its data valid signal. The data accepted signal is then activated by destination unit after it accepts the data from the bus. The source unit then disable its data valid signal which invalidates the data on the bus. After this, the destination unit disables its data accepted signal and the system goes into initial state. The source unit does not send the next data item until after the destination unit shows its readiness to accept new data by disabling the data accepted signal.

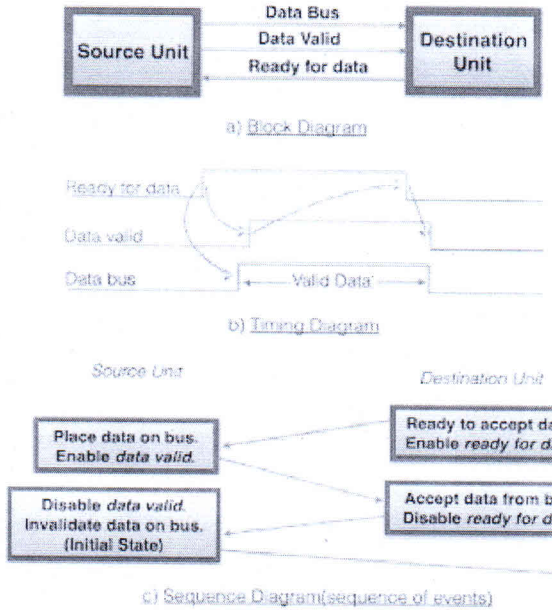
This sequence of events described in its sequence diagram, which shows the above sequence in which the system is present, at any given time

Destination initiated handshaking: The destination-initiated transfer using handshaking lines is shown in figure below:

In its block diagram, we see that the two handshaking lines are "data valid", generated by the source unit, and "ready for data" generated by destination unit. Note that the name of signal data accepted generated by destination unit has been changed to ready for data to reflect its new meaning.

In it, transfer is initiated by destination, so source unit does not place data on data bus until it receives ready for data signal from destination unit. After that, hand shaking process is some as that of source initiated. The sequence of event in it are shown in its sequence diagram and timing relationship between signals is shown in its timing diagram.

Thus, here we can say that, sequence of events in both cases would be identical. If we consider ready for data signal as the complement of data accept. Means, the only difference between source and destination initiated transfer is in their choice of initial state.



In Pursuit of Excellence	Class Test Attendance	SESSION-2019-2020 SEM- 3rd

CT1 Attendance

Section A

Sno	Roll No	Name	Att.
1	1808210001	AASHISH PAL	P
2	1808210002	ABHAY VARSHNEY	P
3	1808210003	ABHAY PRATAP SINGH	P
4	1808210005	ABHISHEK	P
5	1808210006	ABHISHEK KUMAR	A
6	1808210007	ABHISHEK SHARMA	A
7	1808210009	ACHAL GUPTA	P
8	1808210010	ADARSH UPADHYAY	P
9	1808210011	AHAD NUSRAT	D
10	1808210012	AJENDAR	D
11	1808210013	AKASH BHATNAGAR	A
12	1808210014	AKASH JAUHARI	P
13	1808210015	AKASH KUMAR	P
14	1808210016	AKHIL KUMAR	P
15	1808210017	AKSHITA VERMA	P
16	1808210018	AMAN KUMAR	P
17	1808210019	AMAN VAISH	P
18	1808210020	AMBIKA MALHOTRA	P
19	1808210021	AMIR	P
20	1808210022	AMOL JAIN	D
21	1808210025	ANIKET SINGH	P
22	1808210026	ANIL KUMAR	P
23	1808210027	ANIL KUMAR	P
24	1808210028	ANKIT CHANDRA	P
25	1808210029	ANKIT KUMAR	P
26	1808210030	ANKUSH TYAGI	P
27	1808210031	ANSHDEEP TYAGI	A
28	1808210032	ANSHIKA GOEL	A
29	1808210033	ANUBHAV MISHRA	P
30	1808210034	ANUBHAV SHUKLA	P
31	1808210036	ASEEM GUPTA	P
32	1808210037	AVNISH KUMAR	P
33	1808210038	AYUSH KUMAR SINGH	P
34	1808210039	AYUSH SHARMA	P
35	1808210040	BHASKAR SAINI	P

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36	1808210041	BHUVNESH KUMAR SHARMA	P
37	1808210042	BILAL SAIFI	P
38	1808210043	BOBI KHAN	D
39	1808210044	CHANDR VEER SINGH	P
40	1808210046	DEEKSHA SINGH	P
41	1808210047	DEEPENDRA SINGH RAGHAV	P
42	1808210048	DEVAL JHINGRAN	P
43	1808210050	DEVESH BHARDWAJ	P
44	1808210051	GAGAN	P
45	1808210052	GARVIT BHOLA	P
46	1808210053	GAURANG GUPTA	P
47	1808210054	GAURANGEE BHARDWAJ	P
48	1808210055	GAURAV BHATNAGAR	A
49	1808210056	GAURAV KUMAR	P
50	1808210057	GEETIKA GUPTA	P
51	1808210058	HAMMAD HUSSAIN	P
52	1808210059	HARSH GUPTA	P
53	1808210060	HARSH VARDHAN	A
54	1808210061	HARSHBEER SINGH	P
55	1808210062	HARSHIT KUMAR	A
56	1808210063	HARSHIT PANDEY	A
57	1808210064	HONEY TYAGI	P
58	1808210066	IRAM RAFI	P
59	1808210067	ISHAN SAXENA	P

Section C

Sno	Roll No	Name	Att
1	1808210131	SANKALP GUPTA	P
2	1808210132	SANSKRITI AGARWAL	P
3	1808210133	SARTHAK SAXENA	P
4	1808210134	SATAKSHI	P
5	1808210135	SAURABH KUMAR	P
6	1808210136	SAYYDUL MILLAT	D
7	1808210137	SHAZAR ZAIDI	P
8	1808210138	SHIVANI TYAGI	D
9	1808210139	SHIVANSH MATHUR	P
10	1808210140	SHIVANSH AGARWAL	P
11	1808210141	SHIVANSHU AGARWAL	P
12	1808210142	SHREY RUHELA	P
13	1808210143	SHREYA CHAUHAN	P
14	1808210144	SHUBH BHATNAGAR	P
15	1808210146	SHUBHAM YADAV	P
16	1808210147	SHUBHIKA SINGH	P

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17	1808210148	SOURABH SAINI	P
18	1808210149	SPARSH RASTOGI	P
19	1808210150	SRIJAN PANDEY	P
20	1808210151	SUFIYA	P
21	1808210152	SUHAIL AHMED	D
22	1808210153	SUKRITI SINGH	P
23	1808210154	SUMIT KUMAR	P
24	1808210155	SUSHANT KUMAR	P
25	1808210156	SUSHANT SINGH	A
26	1808210157	TANVEER ALAM	P
27	1808210158	UDIT RAJPUT	P
28	1808210159	UMANG MATHUR	P
29	1808210160	UNNATI GANGWAR	P
30	1808210161	UNNATI SINGH	P
31	1808210162	UTKARSH GUPTA	P
32	1808210164	VASU GOEL	P
33	1808210165	VASUNDHRA GUPTA	P
34	1808210166	VEDIKA AGARWAL	P
35	1808210167	VINAYAK VARSHNEY	P
36	1808210168	VIRENDRA MOHAN	P
37	1808210170	VISHAL TYAGI	P
38	1808210171	YASH AGARWAL	P
39	1808210172	ZAMAN ABBAS	D
40		ANUJ SHARMA	P
41		UDIT	P
42		SATYAM RASTOGI	P
43		ZAREEN AQIQ	P
44		VISHAL SAINI	P
45		HADIYA KHALEEQ	P

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CT2 Attendance

Section A

Sno	Roll No	Name	Att
1	1808210001	AASHISH PAL	P
2	1808210002	ABHAY VARSHNEY	P
3	1808210003	ABHAY PRATAP SINGH	P
4	1808210005	ABHISHEK	P
5	1808210006	ABHISHEK KUMAR	P
6	1808210007	ABHISHEK SHARMA	P
7	1808210009	ACHAL GUPTA	P
8	1808210010	ADARSH UPADHYAY	P
9	1808210011	AHAD NUSRAT	P
10	1808210012	AJENDAR	D
11	1808210013	AKASH BHATNAGAR	P
12	1808210014	AKASH JAUHARI	A
13	1808210015	AKASH KUMAR	P
14	1808210016	AKHIL KUMAR	P
15	1808210017	AKSHITA VERMA	P
16	1808210018	AMAN KUMAR	P
17	1808210019	AMAN VAISH	P
18	1808210020	AMBIKA MALHOTRA	P
19	1808210021	AMIR	P
20	1808210022	AMOL JAIN	P
21	1808210025	ANIKET SINGH	P
22	1808210026	ANIL KUMAR	P
23	1808210027	ANIL KUMAR	P
24	1808210028	ANKIT CHANDRA	P
25	1808210029	ANKIT KUMAR	P
26	1808210030	ANKUSH TYAGI	P
27	1808210031	ANSHDEEP TYAGI	P
28	1808210032	ANSHIKA GOEL	P
29	1808210033	ANUBHAV MISHRA	P
30	1808210034	ANUBHAV SHUKLA	P
31	1808210036	ASEEM GUPTA	P
32	1808210037	AVNISH KUMAR	P
33	1808210038	AYUSH KUMAR SINGH	P
34	1808210039	AYUSH SHARMA	P
35	1808210040	BHASKAR SAINI	P
36	1808210041	BHUVNESH KUMAR SHARMA	P
37	1808210042	BILAL SAIFI	P
38	1808210043	BOBI KHAN	D

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39	1808210044	CHANDR VEER SINGH	P
40	1808210046	DEEKSHA SINGH	A
41	1808210047	DEEPENDRA SINGH RAGHAV	A
42	1808210048	DEVAL JHINGRAN	P
43	1808210050	DEVESH BHARDWAJ	P
44	1808210051	GAGAN	P
45	1808210052	GARVIT BHOLA	P
46	1808210053	GAURANG GUPTA	P
47	1808210054	GAURANGEE BHARDWAJ	P
48	1808210055	GAURAV BHATNAGAR	P
49	1808210056	GAURAV KUMAR	P
50	1808210057	GEETIKA GUPTA	P
51	1808210058	HAMMAD HUSSAIN	P
52	1808210059	HARSH GUPTA	P
53	1808210060	HARSH VARDHAN	P
54	1808210061	HARSHBEER SINGH	P
55	1808210062	HARSHIT KUMAR	P
56	1808210063	HARSHIT PANDEY	P
57	1808210064	HONEY TYAGI	P
58	1808210066	IRAM RAFI	P
59	1808210067	ISHAN SAXENA	P

Section C

Sno	Roll No	Name	Att
1	1808210131	SANKALP GUPTA	P
2	1808210132	SANSKRITI AGARWAL	P
3	1808210133	SARTHAK SAXENA	A
4	1808210134	SATAKSHI	P
5	1808210135	SAURABH KUMAR	P
6	1808210136	SAYYDUL MILLAT	P
7	1808210137	SHAZAR ZAIDI	P
8	1808210138	SHIVANI TYAGI	P
9	1808210139	SHIVANSH MATHUR	P
10	1808210140	SHIVANSH AGARWAL	P
11	1808210141	SHIVANSHU AGARWAL	P
12	1808210142	SHREY RUHELA	P
13	1808210143	SHREYA CHAUHAN	P
14	1808210144	SHUBH BHATNAGAR	A
15	1808210146	SHUBHAM YADAV	P
16	1808210147	SHUBHIKA SINGH	P
17	1808210148	SOURABH SAINI	P
18	1808210149	SPARSH RASTOGI	P
19	1808210150	SRIJAN PANDEY	A
20	1808210151	SUFIYA	P

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21	1808210152	SUHAIL AHMED	P
22	1808210153	SUKRITI SINGH	P
23	1808210154	SUMIT KUMAR	P
24	1808210155	SUSHANT KUMAR	P
25	1808210156	SUSHANT SINGH	P
26	1808210157	TANVEER ALAM	P
27	1808210158	UDIT RAJPUT	P
28	1808210159	UMANG MATHUR	P
29	1808210160	UNNATI GANGWAR	P
30	1808210161	UNNATI SINGH	P
31	1808210162	UTKARSH GUPTA	P
32	1808210164	VASU GOEL	A
33	1808210165	VASUNDHRA GUPTA	P
34	1808210166	VEDIKA AGARWAL	P
35	1808210167	VINAYAK VARSHNEY	P
36	1808210168	VIRENDRA MOHAN	P
37	1808210170	VISHAL TYAGI	A
38	1808210171	YASH AGARWAL	P
39	1808210172	ZAMAN ABBAS	P
40		ANUJ SHARMA	P
41		UDIT	P
42		SATYAM RASTOGI	P
43		ZAREEN AQIQ	A
44		VISHAL SAINI	P
45		HADIYA KHALEEQ	P

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CT3 Attendance

Section A

Sno	Roll No	Name	Att
1	1808210001	AASHISH PAL	P
2	1808210002	ABHAY VARSHNEY	P
3	1808210003	ABHAY PRATAP SINGH	P
4	1808210005	ABHISHEK	P
5	1808210006	ABHISHEK KUMAR	P
6	1808210007	ABHISHEK SHARMA	P
7	1808210009	ACHAL GUPTA	P
8	1808210010	ADARSH UPADHYAY	P
9	1808210011	AHAD NUSRAT	P
10	1808210012	AJENDAR	A
11	1808210013	AKASH BHATNAGAR	P
12	1808210014	AKASH JAUHARI	P
13	1808210015	AKASH KUMAR	P
14	1808210016	AKHIL KUMAR	A
15	1808210017	AKSHITA VERMA	P
16	1808210018	AMAN KUMAR	A
17	1808210019	AMAN VAISH	A
18	1808210020	AMBIKA MALHOTRA	P
19	1808210021	AMIR	P
20	1808210022	AMOL JAIN	P
21	1808210025	ANIKET SINGH	A
22	1808210026	ANIL KUMAR	A
23	1808210027	ANIL KUMAR	P
24	1808210028	ANKIT CHANDRA	P
25	1808210029	ANKIT KUMAR	P
26	1808210030	ANKUSH TYAGI	P
27	1808210031	ANSHDEEP TYAGI	P
28	1808210032	ANSHIKA GOEL	P
29	1808210033	ANUBHAV MISHRA	P
30	1808210034	ANUBHAV SHUKLA	P
31	1808210036	ASEEM GUPTA	P
32	1808210037	AVNISH KUMAR	P
33	1808210038	AYUSH KUMAR SINGH	P
34	1808210039	AYUSH SHARMA	P
35	1808210040	BHASKAR SAINI	P
36	1808210041	BHUVNESH KUMAR SHARMA	P
37	1808210042	BILAL SAIFI	P
38	1808210043	BOBI KHAN	P

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39	1808210044	CHANDR VEER SINGH	P
40	1808210046	DEEKSHA SINGH	P
41	1808210047	DEEPENDRA SINGH RAGHAV	P
42	1808210048	DEVAL JHINGRAN	P
43	1808210050	DEVESH BHARDWAJ	P
44	1808210051	GAGAN	P
45	1808210052	GARVIT BHOLA	P
46	1808210053	GAURANG GUPTA	P
47	1808210054	GAURANGEE BHARDWAJ	P
48	1808210055	GAURAV BHATNAGAR	P
49	1808210056	GAURAV KUMAR	P
50	1808210057	GEETIKA GUPTA	P
51	1808210058	HAMMAD HUSSAIN	P
52	1808210059	HARSH GUPTA	P
53	1808210060	HARSH VARDHAN	P
54	1808210061	HARSHBEER SINGH	A
55	1808210062	HARSHIT KUMAR	P
56	1808210063	HARSHIT PANDEY	P
57	1808210064	HONEY TYAGI	A
58	1808210066	IRAM RAFI	A
59	1808210067	ISHAN SAXENA	P

Section C

Sno	Roll No	Name	Att
1	1808210131	SANKALP GUPTA	P
2	1808210132	SANSKRITI AGARWAL	P
3	1808210133	SARTHAK SAXENA	P
4	1808210134	SATAKSHI	A
5	1808210135	SAURABH KUMAR	P
6	1808210136	SAYYDUL MILLAT	P
7	1808210137	SHAZAR ZAIDI	P
8	1808210138	SHIVANI TYAGI	P
9	1808210139	SHIVANSH MATHUR	P
10	1808210140	SHIVANSH AGARWAL	P
11	1808210141	SHIVANSHU AGARWAL	P
12	1808210142	SHREY RUHELA	P
13	1808210143	SHREYA CHAUHAN	P
14	1808210144	SHUBH BHATNAGAR	P
15	1808210146	SHUBHAM YADAV	P
16	1808210147	SHUBHIKA SINGH	P
17	1808210148	SOURABH SAINI	P
18	1808210149	SPARSH RASTOGI	A
19	1808210150	SRIJAN PANDEY	P
20	1808210151	SUFIYA	P

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21	1808210152	SUHAIL AHMED	P
22	1808210153	SUKRITI SINGH	P
23	1808210154	SUMIT KUMAR	P
24	1808210155	SUSHANT KUMAR	P
25	1808210156	SUSHANT SINGH	P
26	1808210157	TANVEER ALAM	P
27	1808210158	UDIT RAJPUT	P
28	1808210159	UMANG MATHUR	A
29	1808210160	UNNATI GANGWAR	P
30	1808210161	UNNATI SINGH	P
31	1808210162	UTKARSH GUPTA	A
32	1808210164	VASU GOEL	P
33	1808210165	VASUNDHRA GUPTA	P
34	1808210166	VEDIKA AGARWAL	P
35	1808210167	VINAYAK VARSHNEY	P
36	1808210168	VIRENDRA MOHAN	P
37	1808210170	VISHAL TYAGI	P
38	1808210171	YASH AGARWAL	P
39	1808210172	ZAMAN ABBAS	P
40		ANUJ SHARMA	P
41		UDIT	P
42		SATYAM RASTOGI	P
43		ZAREEN AQIQ	P
44		VISHAL SAINI	P
45		HADIYA KHALEEQ	P

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In Pursuit of Excellence	List of Students having short attendance	SESSION-2019-2020 SEM- 3rd

KCS302: Computer Organization & Architecture

Till CT1

Section A

Attendance Register. Dates From: 01-08-2019 to 11-09-2019							
Paper Code - KCS-302							
• Course: B.Tech • Year: 2nd • Section: A | Staff Name: Praveen Saini							
S. No.	**Name**	**Student Id**	**Roll Number**	**(P)**	**(A)**	**Tot.**	**Tot. (%age)**
1	Adarsh Upadhayay	1810147	1808210010	10	8	18	55.56
2	Ahad Nusrat	1810253	1808210011	10	8	18	55.56
3	Amir	1810034	1808210021	9	9	18	50
4	Amol Jain	1810194	1808210022	8	10	18	44.44
5	Bobi Khan	1810079	1808210043	8	11	19	42.11

Section C

Attendance Register. Dates From: 01-08-2019 to 11-09-2019							
Paper Code - KCS-302							
• Course: B.Tech • Year: 2nd • Section: C | Staff Name: Praveen Saini							
S. No.	**Name**	**Student Id**	**Roll Number**	**(P)**	**(A)**	**Tot.**	**Tot. (%age)**
1	Sayydul Millat	1810153	1808210136	10	10	20	50
2	Shivani Tyagi	1810261	1808210138	10	10	20	50
3	Suhail Ahmed	1810222	1808210152	7	11	18	38.89
4	Sukirti Singh	1810057	1808210153	9	9	18	50
5	Vasu Goel	1810014	1808210164	8	10	18	44.44
6	Zaman Abbas	1810169	1808210172	8	10	18	44.44
7	Hadiya Khaleeq	2191021	1900820109002	10	8	18	55.56
8	Zareen Aqiq	2191011	1900820109005	10	8	18	55.56

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After CT1 Till CT2

Section A

Attendance Register. Dates From: 15-09-2019 to 21-10-2019							
Paper Code - KCS-302							
• Course: B.Tech • Year: 2nd • Section: A | Staff Name: Praveen Saini							
S. No.	**Name**	**Student Id**	**Roll Number**	**(P)**	**(A)**	**Tot.**	**Tot. (%age)**
1	Aman Kumar	1810271	1808210018	9	10	19	47.37
2	Ankit Kumar	1810211	1808210029	7	11	18	38.89
3	Anshdeep Tyagi	1810013	1808210031	4	14	18	22.22
4	Bhaskar Saini	1810241	1808210040	10	8	18	55.56
5	Gaurang Gupta	1810011	1808210053	11	8	19	57.89
6	Harshit Kumar	1810226	1808210062	11	8	19	57.89

Section C

Attendance Register. Dates From: 15-09-2019 to 21-10-2019							
Paper Code - KCS-302							
• Course: B.Tech • Year: 2nd • Section: C | Staff Name: Praveen Saini							
S. No.	**Name**	**Student Id**	**Roll Number**	**(P)**	**(A)**	**Tot.**	**Tot. (%age)**
1	Sanskriti Agarwal	1810125	1808210132	8	7	15	53.33
2	Sarthak Saxena	1810184	1808210133	8	7	15	53.33
3	Satakshi	1810149	1808210134	6	9	15	40
4	Shivansh Mathur	1810113	1808210139	8	7	15	53.33
5	Sushant Singh	1810100	1808210156	8	8	16	50
6	Unnati Gangwar	1810161	1808210160	4	12	16	25
7	Vishal Saini	2191016	1900820108001	10	7	17	58.82

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In Pursuit of Excellence	**Class Test Marks**	SESSION-2019-2020
		SEM- 3rd

KCS302: Computer Organization & Architecture

CT-1

Section A

Sno	Roll No	Name	CO1						CO2	Total(15)
			Q1(1)	Q2(2)	Q3(2)	Q4(2)	Q5(2)	Q6(3)	Q7(3)	
1	1808210001	AASHISH PAL	0.5	0	2	0.75	1.5	0	0	4.75
2	1808210002	ABHAY VARSHNEY	1	1.75	2	2	1.5	2	1	11.25
3	1808210003	ABHAY PRATAP SINGH	1	0.5	2	0		2	1	6.5
4	1808210005	ABHISHEK	0.75	0.5	2			2	0.25	5.5
5	1808210006	ABHISHEK KUMAR								A
6	1808210007	ABHISHEK SHARMA								A
7	1808210009	ACHAL GUPTA	1	2	0	2	1.5		0.25	6.75
8	1808210010	ADARSH UPADHYAY	1	1.5	2			0		4.5
9	1808210011	AHAD NUSRAT								D
10	1808210012	AJENDAR								D
11	1808210013	AKASH BHATNAGAR								A
12	1808210014	AKASH JAUHARI	0.75		1		1.75	2		5.5
13	1808210015	AKASH KUMAR	1	2	2	0	0.5	1.75	1	8.25
14	1808210016	AKHIL KUMAR	1	0.75	2	0.5	0.25	2	1	7.5
15	1808210017	AKSHITA VERMA	1	0	2	0	1.5	1.75	0	6.25
16	1808210018	AMAN KUMAR	1	1.5	1.5		1.5	1.75		7.25
17	1808210019	AMAN VAISH	1	0.5	0.5	1.75		0.5		4.25
18	1808210020	AMBIKA MALHOTRA	1	2	0.75	1.25	1.5	2	1.5	10
19	1808210021	AMIR	0.75	2	1.5	0.5	0.5	0.5	0.5	6.25
20	1808210022	AMOL JAIN								D
21	1808210025	ANIKET SINGH	1	0.75	2	1	0.5	2		7.25
22	1808210026	ANIL KUMAR	1	0.25	2	0	0.5	0.5	0	4.25
23	1808210027	ANIL KUMAR	1	0	2		0.5	0.5	0.5	4.5
24	1808210028	ANKIT CHANDRA	0.75	0.75	2			1	0.5	5
25	1808210029	ANKIT KUMAR	0.75		1.5	0.5	0.5			3.25
26	1808210030	ANKUSH TYAGI	1	0.25	1	0	1.5	0.25	0	4
27	1808210031	ANSHDEEP TYAGI								A
28	1808210032	ANSHIKA GOEL								A
29	1808210033	ANUBHAV MISHRA	1	0	2	0.75				3.75

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30	1808210034	ANUBHAV SHUKLA	1	0	2	1.25	0.25			4.5
31	1808210036	ASEEM GUPTA	1	0.5	0.5	0	1.5	2	0	5.5
32	1808210037	AVNISH KUMAR	1	0			0.75			1.75
33	1808210038	AYUSH KUMAR SINGH	1	2	2					5
34	1808210039	AYUSH SHARMA	1	1.5	0	2	1.5	1.75	0	7.75
35	1808210040	BHASKAR SAINI	1	0.5	0.75	2	0.5	0.75		5.5
36	1808210041	BHUVNESH KUMAR SHARMA	1	0	2	0	0.25	2	0	5.25
37	1808210042	BILAL SAIFI	1	0	2		0	1.5		4.5
38	1808210043	BOBI KHAN								D
39	1808210044	CHANDR VEER SINGH	1	0	2			2		5
40	1808210046	DEEKSHA SINGH	1		2		0	1.75	0	4.75
41	1808210047	DEEPENDRA SINGH RAGHAV	1	2	1.75		0	2.75		7.5
42	1808210048	DEVAL JHINGRAN	1	2	2	0.5	2	2.75	0.5	10.75
43	1808210050	DEVESH BHARDWAJ	1	0.25	2	2	2		0	7.25
44	1808210051	GAGAN	1	0	0.5		0.25		0	1.75
45	1808210052	GARVIT BHOLA	1	0.25	2	0.5	1.5	0		5.25
46	1808210053	GAURANG GUPTA	1	0.25	2	0	0	0	0	3.25
47	1808210054	GAURANGEE BHARDWAJ	1	1	2	0.25	1.5	2	0.5	8.25
48	1808210055	GAURAV BHATNAGAR								A
49	1808210056	GAURAV KUMAR	1	0	0.5	0.25	0	0.25	0	2
50	1808210057	GEETIKA GUPTA	1	1.5	2	2	1.5	1.5	1	10.5
51	1808210058	HAMMAD HUSSAIN	1	0			0.5	2.75		4.25
52	1808210059	HARSH GUPTA	1	0	2		2	2.5	0.5	8
53	1808210060	HARSH VARDHAN								A
54	1808210061	HARSHBEER SINGH	1	2	2	2	2	2.5	3	14.5
55	1808210062	HARSHIT KUMAR								A
56	1808210063	HARSHIT PANDEY								A
57	1808210064	HONEY TYAGI	1		0.5			2		3.5
58	1808210066	IRAM RAFI	1	0.5	2	0	1.5	2	3	10
59	1808210067	ISHAN SAXENA	1	0	2	0	0	2		5

Section C

			CO1						CO2	
Sno	**Roll No**	**Name**	**Q1(1)**	**Q2(2)**	**Q3(2)**	**Q4(2)**	**Q5(2)**	**Q6(3)**	**Q7(3)**	**Total(15)**
1	1808210131	SANKALP GUPTA	1	0.25	0.25	0	0.25	2	0.5	4.25
2	1808210132	SANSKRITI AGARWAL	1	1.25	2	2	1.75	2	0.5	10.5
3	1808210133	SARTHAK SAXENA	1		1.75			2	0.5	5.25
4	1808210134	SATAKSHI	1	0	1.75	0.75	0	2	0.5	6
5	1808210135	SAURABH KUMAR	1	0	1.5	2	0	2	0	6.5
6	1808210136	SAYYDUL MILLAT								D
7	1808210137	SHAZAR ZAIDI	1	0		0.25	0	1.75	0.25	3.25
8	1808210138	SHIVANI TYAGI								D
9	1808210139	SHIVANSH MATHUR	1	1.5	1.75	1.75	0.25	2.75	0.5	9.5
10	1808210140	SHIVANSH AGARWAL	1	0.25	1	0	1.5	1.5	0	5.25

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11	1808210141	SHIVANSHU AGARWAL	1	0.25	1.5		0.75		0.5	4
12	1808210142	SHREY RUHELA	1	0.5	0.5	0	0	0.25		2.25
13	1808210143	SHREYA CHAUHAN	1	1.25	1.25	0		1	0	4.5
14	1808210144	SHUBH BHATNAGAR	0.5	0.5	2	0	0	2	0	5
15	1808210146	SHUBHAM YADAV	0.25	0.5	2	0.75	0	2	0.5	6
16	1808210147	SHUBHIKA SINGH	1	1	1.5	0	0	1.75	0	5.25
17	1808210148	SOURABH SAINI	1	1.75	0.5	1		0	1.5	5.75
18	1808210149	SPARSH RASTOGI	1	0.5	2		1			4.5
19	1808210150	SRIJAN PANDEY	0.75		2		0.75		0.25	3.75
20	1808210151	SUFIYA	1	1	2	2	2	2.75	0.75	11.5
21	1808210152	SUHAIL AHMED								D
22	1808210153	SUKRITI SINGH	0.5	0	1.5	2	1.5	2	0.25	7.75
23	1808210154	SUMIT KUMAR	1				0	2	0.5	3.5
24	1808210155	SUSHANT KUMAR	1	1	1	0	1.25	1.75	0	6
25	1808210156	SUSHANT SINGH								A
26	1808210157	TANVEER ALAM	1	2	1	1		0.5	0.5	6
27	1808210158	UDIT RAJPUT	1	0.5	1.5	2	1.5	2	0.5	9
28	1808210159	UMANG MATHUR	1			1.5	0	2	0	4.5
29	1808210160	UNNATI GANGWAR	1	0.5	1.5	0.75	0.75	1.75		6.25
30	1808210161	UNNATI SINGH	1	0.75		0.5	0	2		4.25
31	1808210162	UTKARSH GUPTA	1	0.5	2	0	1.5	2.5		7.5
32	1808210164	VASU GOEL	1	1.75	2		0.5	2.75		8
33	1808210165	VASUNDHRA GUPTA	1	1.25	2	0.75	0	1.75		6.75
34	1808210166	VEDIKA AGARWAL	1	1.25	2	0.75	0	1.75		6.75
35	1808210167	VINAYAK VARSHNEY	1	1.75	1	0	2	2.75	0.5	9
36	1808210168	VIRENDRA MOHAN	1	0.75	1.5			2	0.25	5.5
37	1808210170	VISHAL TYAGI	1	0.75	1	0.25	0	2	0	5
38	1808210171	YASH AGARWAL	1	1.25	1	0.25	0	2	0	5.5
39	1808210172	ZAMAN ABBAS								D
40		ANUJ SHARMA	1	0.5	1	0.25	1.75	0.5		5
41		UDIT	1	1.75	2	0	0.5			5.25
42		SATYAM RASTOGI	1	1.25			1	2		5.25
43		ZAREEN AQIQ	1		1.5	1	1	0.5		5
44		VISHAL SAINI	1	0.75	0.75	0	1.75	2		6.25
45		HADIYA KHALEEQ	1	0	1	0	0.5	1.75		4.25

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Section A

Sno	Roll No	Name	CO2				CO3		Total(15)
			Q1(2)	Q2(2)	Q3(2)	Q4(3)	Q5(3)	Q6(3)	
1	1808210001	AASHISH PAL	0.5	0.25	0.5	1	1.75	3	7
2	1808210002	ABHAY VARSHNEY	1.5	2	0.5	3	3	3	13
3	1808210003	ABHAY PRATAP SINGH	0.5	0.25	0.5	0.25	1.5	3	6
4	1808210005	ABHISHEK	2		0.25		1		3.25
5	1808210006	ABHISHEK KUMAR	0.25	0.25	0.25	0.25	2.25	0	3.25
6	1808210007	ABHISHEK SHARMA	2	2	1.5	2.75	3	2	13.25
7	1808210009	ACHAL GUPTA	0.5	1.75	1.25	0.5	2.5	2	8.5
8	1808210010	ADARSH UPADHYAY	0.5	1.75		2.75	0.5	3	8.5
9	1808210011	AHAD NUSRAT	0		0	2		3	5
10	1808210012	AJENDAR							D
11	1808210013	AKASH BHATNAGAR	1.25	0.25	2	3	3	3	12.5
12	1808210014	AKASH JAUHARI							A
13	1808210015	AKASH KUMAR	1.5	2	0.5	0.5	3	0.5	8
14	1808210016	AKHIL KUMAR	0.5	0	0.5	0.5	1	1	3.5
15	1808210017	AKSHITA VERMA	1.75	2	0.25	1	3	1	9
16	1808210018	AMAN KUMAR	0.5	0.25	0.25	1	2.5		4.5
17	1808210019	AMAN VAISH	1.75	1		1	2.25		6
18	1808210020	AMBIKA MALHOTRA	1.75	2	2	3	3	1	12.75
19	1808210021	AMIR	0	1	0.25	0.25	0.25		1.75
20	1808210022	AMOL JAIN	0.5	1.25		2.5	2.5		6.75
21	1808210025	ANIKET SINGH	0.75		0.25		2	0.25	3.25
22	1808210026	ANIL KUMAR	1.25	1.75	0.5	0.5	2.25	0.25	6.5
23	1808210027	ANIL KUMAR		0	0.25		0	0.25	0.5
24	1808210028	ANKIT CHANDRA		0.75	1	0.75	0		2.5
25	1808210029	ANKIT KUMAR			0.75	0.75	2.25		3.75
26	1808210030	ANKUSH TYAGI	0.5	0.25	0.75	0.5	2.5	0.25	4.75
27	1808210031	ANSHDEEP TYAGI	1	0.5	0.5	0	2		4
28	1808210032	ANSHIKA GOEL	0.25	1	1.25	0.5	2.5	1.25	6.75
29	1808210033	ANUBHAV MISHRA	0.5	1.25	1.25	1.75	2.25		7
30	1808210034	ANUBHAV SHUKLA	0.5	2	1.75	0.5	2.25	0	7
31	1808210036	ASEEM GUPTA	0.25	2	0	0.25	1.5	1	5
32	1808210037	AVNISH KUMAR	1	2	0.25	3	1.5		7.75
33	1808210038	AYUSH KUMAR SINGH			0.25	0.25			0.5
34	1808210039	AYUSH SHARMA	1.25	2		2.75	3	1	10
35	1808210040	BHASKAR SAINI	0.25	0		0.25	1		1.5
36	1808210041	BHUVNESH KUMAR SHARMA	1.5	2	2	3	2.5	1	12
37	1808210042	BILAL SAIFI	1	0.25		0.75	2.5	0	4.5
38	1808210043	BOBI KHAN							D
39	1808210044	CHANDR VEER SINGH	1.5			3	0		4.5

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40	1808210046	DEEKSHA SINGH							A
41	1808210047	DEEPENDRA SINGH RAGHAV							A
42	1808210048	DEVAL JHINGRAN	1.25	2	0.5	0.5	3		7.25
43	1808210050	DEVESH BHARDWAJ	2	2	0.5	3	3	1	11.5
44	1808210051	GAGAN			0.75	0.75		1	2.5
45	1808210052	GARVIT BHOLA	2	0.5	2	3	3	2	12.5
46	1808210053	GAURANG GUPTA	0.5	0.75	0.5	0.25	0	0	2
47	1808210054	GAURANGEE BHARDWAJ	1.5	2	1.75	1.5	2.5	3	12.25
48	1808210055	GAURAV BHATNAGAR	0.75		0.25	0.25	2	2	5.25
49	1808210056	GAURAV KUMAR	2	0.5	0.5	0.5	1	1.5	6
50	1808210057	GEETIKA GUPTA	1.5	2	0.5	3	3	1	11
51	1808210058	HAMMAD HUSSAIN	0			0.25	2.25		2.5
52	1808210059	HARSH GUPTA	2	1.75	0.25	3	3	3	13
53	1808210060	HARSH VARDHAN	2	0.25	0.5	0.5	2.25	3	8.5
54	1808210061	HARSHBEER SINGH	2	2	2	2.75	3	3	14.75
55	1808210062	HARSHIT KUMAR	0.75	0		1.75	0		2.5
56	1808210063	HARSHIT PANDEY	0.25	2	0.5	0.25	3	2	8
57	1808210064	HONEY TYAGI	2	2	0.5	3	3	2	12.5
58	1808210066	IRAM RAFI	2	2	1.5	1	2	0	8.5
59	1808210067	ISHAN SAXENA	2	2	2	1	3		10

Section C

			CO2				CO3		
Sno	**Roll No**	**Name**	**Q1(2)**	**Q2(2)**	**Q3(2)**	**Q4(3)**	**Q5(3)**	**Q6(3)**	**Total(15)**
1	1808210131	SANKALP GUPTA	1.25	0.75	0.5	0.5	3		6
2	1808210132	SANSKRITI AGARWAL	2	2	2	2.25	3	1.25	12.5
3	1808210133	SARTHAK SAXENA							A
4	1808210134	SATAKSHI	1.75	0.25	0.75	0	2	1	5.75
5	1808210135	SAURABH KUMAR	2	0.5	0.75	3	2		8.25
6	1808210136	SAYYDUL MILLAT		0.5			2.5		3
7	1808210137	SHAZAR ZAIDI		0		0.5	1		1.5
8	1808210138	SHIVANI TYAGI	0		0.75	0.5	2	2	5.25
9	1808210139	SHIVANSH MATHUR		2	2	1	1.5	1	7.5
10	1808210140	SHIVANSH AGARWAL	1.75	2	1.25	3	3	0	11
11	1808210141	SHIVANSHU AGARWAL		1.5	0.75	1	1	1	5.25
12	1808210142	SHREY RUHELA	0.5	0.75	1.25	0.25	0.25	0.5	3.5
13	1808210143	SHREYA CHAUHAN		0.5		0	1.5	0	2
14	1808210144	SHUBH BHATNAGAR							A
15	1808210146	SHUBHAM YADAV	0.25	2	0.25	0.5	2.75		5.75
16	1808210147	SHUBHIKA SINGH		0.25	0.25		3	0	3.5
17	1808210148	SOURABH SAINI		0.75		0	2.5		3.25
18	1808210149	SPARSH RASTOGI	1.5			3	3		7.5
19	1808210150	SRIJAN PANDEY							A
20	1808210151	SUFIYA	2	2	1.75	3	3	1	12.75

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21	1808210152	SUHAIL AHMED	1	0.5			1.5	0	3
22	1808210153	SUKRITI SINGH	0.25	0.75	0.25				1.25
23	1808210154	SUMIT KUMAR	1.5	1.25		3	2.25		8
24	1808210155	SUSHANT KUMAR	0.5	0.5	0.5	0.5	3	0	5
25	1808210156	SUSHANT SINGH		0.25		0.5	2.25	2	5
26	1808210157	TANVEER ALAM	0.75	0.75	0	0.5	2.5		4.5
27	1808210158	UDIT RAJPUT	2	1.5	2	2.75	2.75	1.5	12.5
28	1808210159	UMANG MATHUR	1.75		0	3	1.5		6.25
29	1808210160	UNNATI GANGWAR	0.25	0.25	0	0.5	0		1
30	1808210161	UNNATI SINGH	0.5	0		0.25	1.75	0.25	2.75
31	1808210162	UTKARSH GUPTA	0.5		0.5	1.5	1.5		4
32	1808210164	VASU GOEL							A
33	1808210165	VASUNDHRA GUPTA	0.25	0.75	0.25	0	0.25	0	1.5
34	1808210166	VEDIKA AGARWAL	0	0.25	0.25		0.5		1
35	1808210167	VINAYAK VARSHNEY	2	1	0.25	3	0.5	0	6.75
36	1808210168	VIRENDRA MOHAN	0	0.25	0	0		0	0.25
37	1808210170	VISHAL TYAGI							A
38	1808210171	YASH AGARWAL	0.5	2		0.5	3		6
39	1808210172	ZAMAN ABBAS	2		0.5	1	2.5	1.75	7.75
40		ANUJ SHARMA	0.5	2	0.5	0.25	0.75	0	4
41		UDIT					0		0
42		SATYAM RASTOGI	0.25	0.25	0.25		1.25		2
43		ZAREEN AQIQ							A
44		VISHAL SAINI	0	0.25	0	0	2.25	0.25	2.75
45		HADIYA KHALEEQ	0.25	0.5	1.75	0	1.75	1	5.25

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Section A

Sno	Roll No	Name	CO3		CO5	CO4		CO5	Total(15)
			Q1(2)	Q2(2)	Q3(2)	Q4(3)	Q5(3)	Q6(3)	
1	1808210001	AASHISH PAL	1	1.5	1.5	3	1	0	8
2	1808210002	ABHAY VARSHNEY	2	2	2	2.75	2	0.5	11.25
3	1808210003	ABHAY PRATAP SINGH	2	2	1.75	2.75	1.5	0.5	10.5
4	1808210005	ABHISHEK		1.75	2	3	0.5	0.5	7.75
5	1808210006	ABHISHEK KUMAR	1.5	1.5	1.75	3	1.25	0.5	9.5
6	1808210007	ABHISHEK SHARMA	1	1.75	1.25	3	2.75		9.75
7	1808210009	ACHAL GUPTA	1	1.75	1.75	2.5	2		9
8	1808210010	ADARSH UPADHYAY	0.75	0.25	1	2	3	0.25	7.25
9	1808210011	AHAD NUSRAT	1.5	1	1.5		2	1	7
10	1808210012	AJENDAR							A
11	1808210013	AKASH BHATNAGAR	1.75	2	1.5	3	2	0	10.25
12	1808210014	AKASH JAUHARI	1.75	1.5	1	3	2.5	0.25	10
13	1808210015	AKASH KUMAR	2	2	1.5	3	3	1	12.5
14	1808210016	AKHIL KUMAR							A
15	1808210017	AKSHITA VERMA	0.75	1.25	1.5	2.25	0.25	1	7
16	1808210018	AMAN KUMAR							A
17	1808210019	AMAN VAISH							A
18	1808210020	AMBIKA MALHOTRA	2	2	1.75	3	1.25	2.5	12.5
19	1808210021	AMIR	0.25	1	1.5	2	0.5	0.5	5.75
20	1808210022	AMOL JAIN				3		1.75	4.75
21	1808210025	ANIKET SINGH							A
22	1808210026	ANIL KUMAR							A
23	1808210027	ANIL KUMAR	0	1	0.75	3	0	0.75	5.5
24	1808210028	ANKIT CHANDRA	1.5	0.5	2	0	2.5	0.5	7
25	1808210029	ANKIT KUMAR	2		1.5	2	2.5		8
26	1808210030	ANKUSH TYAGI	1.25	1.75	0.75	3	2	1	9.75
27	1808210031	ANSHDEEP TYAGI	1.5	1.5	1.25	2.5		1.25	8
28	1808210032	ANSHIKA GOEL	1.75	1.75	1	3	1.5		9
29	1808210033	ANUBHAV MISHRA			0.5	2.5	1		4
30	1808210034	ANUBHAV SHUKLA	0	0.5	0.25	1	0	0.5	2.25
31	1808210036	ASEEM GUPTA	1.5	2	2	3	1.25	0.75	10.5
32	1808210037	AVNISH KUMAR	0.75	1.75	0.75	3	0.5	0.75	7.5
33	1808210038	AYUSH KUMAR SINGH	1	1.5		3	1	0.5	7
34	1808210039	AYUSH SHARMA		1	0.5	1.5	0.5	0	3.5
35	1808210040	BHASKAR SAINI		0.5	1	3	0	1.5	6
36	1808210041	BHUVNESH KUMAR SHARMA	2	1.5	1.5	3	2.25	2.75	13
37	1808210042	BILAL SAIFI	1.75	1.5	1.5	2.75	2	0	9.5
38	1808210043	BOBI KHAN	2		1	2.5	2.5	2	10
39	1808210044	CHANDR VEER SINGH		1.5	1.5	2.5	1.5		7

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40	1808210046	DEEKSHA SINGH	2	1.25	1.25	3	1.5		9
41	1808210047	DEEPENDRA SINGH RAGHAV	1.25	1.5	0.75	2	2.25	0.5	8.25
42	1808210048	DEVAL JHINGRAN	1.5	1.75	1.5	3	2.25		10
43	1808210050	DEVESH BHARDWAJ	2	1.75	2	3	2.25		11
44	1808210051	GAGAN	1.75	1.75	1.5	3	2.25		10.25
45	1808210052	GARVIT BHOLA	1.75	2	2	3	2.25	0.25	11.25
46	1808210053	GAURANG GUPTA		1.5	1	3	1	3	9.5
47	1808210054	GAURANGEE BHARDWAJ	1.5	1.75	1	3	3	3	13.25
48	1808210055	GAURAV BHATNAGAR	0.75	2	0.5	3	0.75		7
49	1808210056	GAURAV KUMAR	0.5	1.5	0.5	2.5	0.75	0	5.75
50	1808210057	GEETIKA GUPTA	2	1.75	1.5	2.5	0.75	0.5	9
51	1808210058	HAMMAD HUSSAIN	2	1.25	1.5	1	0.75		6.5
52	1808210059	HARSH GUPTA	2	1.75	2	3	3	0.75	12.5
53	1808210060	HARSH VARDHAN	1	1.25	1	2.5	3	0	8.75
54	1808210061	HARSHBEER SINGH							A
55	1808210062	HARSHIT KUMAR	1.5	0	1.5	1	2.5	2.5	9
56	1808210063	HARSHIT PANDEY	1.5	0.75	0.5	2.5	0.25		5.5
57	1808210064	HONEY TYAGI							A
58	1808210066	IRAM RAFI							A
59	1808210067	ISHAN SAXENA	0.25	0.25	0	3	1		4.5

Section C

			CO3		CO5	CO4		CO5	
Sno	**Roll No**	**Name**	**Q1(2)**	**Q2(2)**	**Q3(2)**	**Q4(3)**	**Q5(3)**	**Q6(3)**	**Total(15)**
1	1808210131	SANKALP GUPTA	1.5	1.5	0.25	3	1.25	2	9.5
2	1808210132	SANSKRITI AGARWAL	1.5	1.75		1.25	0	1	5.5
3	1808210133	SARTHAK SAXENA	1.5	1.75		3			6.25
4	1808210134	SATAKSHI							A
5	1808210135	SAURABH KUMAR	1.5	1.5	1	2.75	1.25	1	9
6	1808210136	SAYYDUL MILLAT	2	2	1.5	3		0.5	9
7	1808210137	SHAZAR ZAIDI	1.75	0.75	0.25	3	0	2.5	8.25
8	1808210138	SHIVANI TYAGI	1.5	1.75	0	3		0.25	6.5
9	1808210139	SHIVANSH MATHUR	1.5	1.75	1	3	1.5	1.25	10
10	1808210140	SHIVANSH AGARWAL	2	1.75	1.75	2	1.5	1	10
11	1808210141	SHIVANSHU AGARWAL	2	0.5	1.5	1	1.75		6.75
12	1808210142	SHREY RUHELA	1.75	1.75	1	2.5	0.25	0	7.25
13	1808210143	SHREYA CHAUHAN	1.75	1.25	1	3	0.5		7.5
14	1808210144	SHUBH BHATNAGAR	1	1.5	1.75	2	0	2.5	8.75
15	1808210146	SHUBHAM YADAV	1	1	1.75	2.5		2.25	8.5
16	1808210147	SHUBHIKA SINGH	1.75	1.5	1.5	2.25	1	0.5	8.5
17	1808210148	SOURABH SAINI			1	1	2	1	5
18	1808210149	SPARSH RASTOGI							A
19	1808210150	SRIJAN PANDEY	1	1	2	2	0	2.25	8.25
20	1808210151	SUFIYA	1.75	2	1	3	1.25	3	12

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21	1808210152	SUHAIL AHMED	2	1.75	0.75	3		1.25	8.75
22	1808210153	SUKRITI SINGH	0.75	1.5	0.75	3	0	1	7
23	1808210154	SUMIT KUMAR	0.75	1.5	2	3		0.5	7.75
24	1808210155	SUSHANT KUMAR	1.5	0.5	0	3	0	0.5	5.5
25	1808210156	SUSHANT SINGH	1	1	1	2.5	0.5	3	9
26	1808210157	TANVEER ALAM	1	1		3	0.25		5.25
27	1808210158	UDIT RAJPUT	2	2	1	3	2.25	2.75	13
28	1808210159	UMANG MATHUR							A
29	1808210160	UNNATI GANGWAR	0	1.5		2.5	0	1.25	5.25
30	1808210161	UNNATI SINGH	1.5		1	3	0.75		6.25
31	1808210162	UTKARSH GUPTA							A
32	1808210164	VASU GOEL			1.5	1	1.5		4
33	1808210165	VASUNDHRA GUPTA		1.75	1.75	3	0	1	7.5
34	1808210166	VEDIKA AGARWAL		1.75	0.25	3		0	5
35	1808210167	VINAYAK VARSHNEY	1.75	1.75	1	1.5	0.75	1	7.75
36	1808210168	VIRENDRA MOHAN		1.75	1.25	2.75	0.5	0	6.25
37	1808210170	VISHAL TYAGI		1.75	1.75	3		1.25	7.75
38	1808210171	YASH AGARWAL	0	1.75	1.75	3	0.5	1.5	8.5
39	1808210172	ZAMAN ABBAS		1.5	1.5	1.25			4.25
40		ANUJ SHARMA			1	3		3	7
41		UDIT		1.5	1.75	3			6.25
42		SATYAM RASTOGI			0.75	3	0	1	4.75
43		ZAREEN AQIQ	1.75	2	0.5	2.25		0.5	7
44		VISHAL SAINI	0	1.5	1.5	3	1.5		7.5
45		HADIYA KHALEEQ	1.5		2	3	0	2.5	9

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In Pursuit of Excellence	**List of Weak Students** (Action taken for Improvement)	SESSION-2019-2020
		SEM- 3rd

KCS302: Computer Organization & Architecture

Section A

Sno	Roll no	Name
1	1808210006	ABHISHEK KUMAR
2	1808210027	ANIL KUMAR
3	1808210029	ANKIT KUMAR
4	1808210031	ANSHDEEP TYAGI
5	1808210042	BILAL SAIFI
6	1808210043	BOBI KHAN
7	1808210051	GAGAN
8	1808210053	GAURANG GUPTA
9	1808210058	HAMMAD HUSSAIN
10	1808210062	HARSHIT KUMAR

Section C

Sno	Roll no	Name
1	1808210136	SAYYDUL MILLAT
2	1808210137	SHAZAR ZAIDI
3	1808210142	SHREY RUHELA
4	1808210143	SHREYA CHAUHAN
5	1808210150	SRIJAN PANDEY
6	1808210152	SUHAIL AHMED
7	1808210161	UNNATI SINGH

Action Taken

1. Special focus in tutorial class via motivation and Q/A discussions.
2. Extra slots assign to them on Saturday 3pm and discussed on Topics "Booth Algorithm, Floating point representation, Control Unit and DMA".
3. Providing a question bank having important question.

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Question Bank for weak students

KCS302: Computer Organization & Architecture

[CO- 1]

1. Explain: Serial Bus Arbitration or Parallel Bus Arbitration.
2. What is stack organization? Compare register stack and memory stack.
3. Convert the following arithmetic expressions from infix to reverse polish notation.
   a. $A * B + C * D + E * F$
   b. $A + B * [C * D + E * (F + G)]$

[CO- 2]

4. Draw the hardware details for the Booth's Multiplication algorithm and using Booth's multiplication multiply decimal numbers (-23) and (+9).
5. Represent (-307.1875)10 in single precision and double precision format.

[CO- 3]

6. Explain all the phases of instruction cycle.
7. Explain the basic concept of Hardwired and Software control unit with neat diagrams. What are the advantages and disadvantages in each control?
8. What is a microprogram sequencer? With block diagram, explain the working of microprogram sequencer.
9. What are the difference between Horizontal and vertical micro codes?
10. Differentiate between RISC & CISC based microprocessor.

[CO- 4]

11. Write the difference between RAM & ROM.
12. Explain memory hierarchy with diagram.
13. Discuss the various types of address mapping used in cache memory.

[CO- 5]

14. What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each?
15. Explain the working of DMA controller with help of suitable diagrams.
16. Write short note on Input Output Processor.

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In Pursuit of Excellence	**List of Bright Students** (Action taken for enhancing performance)	SESSION-2019-2020
		SEM- 3rd

KCS302: Computer Organization & Architecture

Section A

Sno.	Roll no.	Name
1	ABHAY VARSHNEY	1808210002
2	AMBIKA MALHOTRA	1808210020
3	GEETIKA GUPTA	1808210057
4	HARSHBEER SINGH	1808210061
5	IRAM RAFI	1808210066

Section C

Sno.	Roll no.	Name
1	SANSKRITI AGARWAL	1808210132
2	SHIVANSH MATHUR	1808210139
3	SUFIYA	1808210151
4	UDIT RAJPUT	1808210158

Action Taken

1. Discussing Question based on previous year GATE paper on **"Instruction Format"**.
2. Shared NPTEL video lectures: https://nptel.ac.in/courses/106/105/106105163/
3. Shared weblink having gate questions https://gateoverflow.in/co-and-architecture
4. Provided list of Topics those generally asked competitive exams.

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Question asked in GATE from Instruction format

Gate 1992 In an 11-bit computer instruction format, the size of address field is 4 bits. The computer uses expanding OPCODE technique & has 5 two-address instructions & 32 one-address instructions. The number of 0-address instructions it can support is -

A) 512 B) 256 C) 1024 D) None of these

Sol^n: 11 bits instruction, so total instruction = 2^{11} = 2048

Address field = 4 bits

Two-address instruction = $5 \times 2^4 \times 2^4 = 5 \times 16 \times 16 = 80 \times 16 = 1280$

One-address instruction = $32 \times 2^4 = 32 \times 16 = 512$

Zero-address instruction = $2048 - (1280 + 512)$

$= 2048 - 1792$

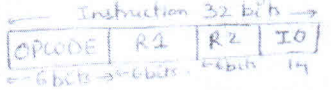
$= 256$

Option B

Gate 2014 A machine has a 32-bit architecture with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instruction which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is -

A) $2^{14}+1$ B) $2^{15}-1$ C) $2^{14}-1$ D) None of these

Sol^n: 32 bits architecture.



64 registers i.e, 6 bits for register number ; Register size = 32 bits

45 instructions i.e, 6 bits

Immediate operand (I0) = 32 - 18 = 14

For unsigned integer, $2^{14}-1$ will be the maximum value

option C

Gate 2016 A processor has 40 distinct instructions & 24 general purpose registers. A 32-bit instruction word has an opcode, two registers operands, & an immediate operand. The number of bits available for the immediate operand field is —

Soln: 40 instructions i.e, no. of bits for opcode = 6 bits
24 register, i.e, no of bits required = 5 bits
Total bits occupied by two registers & 1 opcode = 5+5+6 = 16 bits

As instruction word given is 32 bits, remaining bit left for operand = 32 − 16 = 16 bits

List of Topics from which questions has been asked in competitive examinations

Sno.	Name of Topic
1.	Signed number representation and complements
2.	Floating Point representation
3.	Instruction Format
4.	Cache Memory

In Pursuit of Excellence	**Previous Year Question Papers**	SESSION-2019-2020
		SEM- 3rd

Printed pages: 02

Paper Id: 1 1 0 3 0 2

Roll No.

Sub Code: RCS302

BTECH
(SEM III) THEORY EXAMINATION 2018-19
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours *Total Marks: 70*

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. **Attempt *all* questions in brief.** 2 x 7 = 14

a. What do you understand by Locality of Reference?
b. Which of the following architecture is/are not suitable for realizing SIMD?
c. What is the difference between RAM and DRAM?
d. What are the difference between Horizontal and vertical micro codes?
e. Describe cycle stealing in DMA.
f. List three types of control signals.
g. Define the role of MIMD in computer architecture.

SECTION B

2. **Attempt any *three* of the following:** 7 x 3 = 21

a. Evaluate the arithmetic statement X = (A+B)*(C+D) using a general register computer with three address, two address and one address instruction format a program to evaluate the expression .
b. Perform the division process of 00001111 by 0011(use a dividend of 8 bits).
c. A two way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from memory. The main memory size is 128K X 32.
   i. Formulate all pertinent information required to construct the cache memory.
   ii. What is the size of cache memory?
d. What is associative memory? Explain with the help of a block diagram. Also mention the situation in which associative memory can be effective utilized.
e. A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.
   (i) How many bits are there in the operation code, the register code part and the address part?
   (ii) Draw the instruction word format and indicate the number of bits in each part.
   (iii) How many bits are there in the data and address inputs of the memory?

SECTION C

3. **Attempt any *one* part of the following:** **7 x 1 = 10**

(a) Write short notes on :
(i) Instruction pipeline.
(ii) DMA based data transfer.

(b) Explain the difference between vectored and non-vectored interrupt. Explain stating examples of each.

4. **Attempt any *one* part of the following:** **7x 1 = 10**

(a) Draw the flow chart of Booth's Algorithm for multiplication and show the multiplication process using Booth's Algorithm for (-7) X (+3).

(b) Write short notes on:
(i) Amdahl's Law
(ii) Pipelining

5. **Attempt any *one* part of the following:** **7 x 1 = 10**

(a) What is a microprogram sequencer? With block diagram, explain the working of microprogram sequencer.

(b) Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation.

6. **Attempt any *one* part of the following:** **7 x 1 = 10**

(a) Give the block diagram of DMA controller. Why are the read and write control lines in a DMA controller bidirectional?

(b) Explain all the phases of instruction cycle.

7. **Attempt any *one* part of the following:** **7 x 1 = 10**

(a) Explain the basic concept of Hardwired and Software control unit with neat diagrams.

(b)

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

For the following Reservation table:

i. Calculate the set of the forbidden latencies and collision vector.
ii. Draw a state diagram, showing all possible initial sequences (cycles) without a collision in the pipeline.
iii. Simple cycles (SC)
iv. Greedy cycles among simple the cycles
v. MAL (minimum average latency)
vi. What is the minimum allowed constant cycles
vii. Maxi. Throughput
viii. Throughput if the minimum constant cycle is used.

Printed pages: 02

Sub Code: RCS 302

Paper Id: 1 0 0 3

Roll No.

B.Tech.
(SEM III) THEORY EXAMINATION 2017-18
COMPUTER ORGANIZATION & ARCHITECTURE

Time: 3 Hours *Total Marks: 70*

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. **Attempt *all* questions in brief.** **2 x 7 = 14**
   a. Draw the circuit diagram of D Flip Flop.
   b. Write the difference between RAM & ROM.
   c. Write short note on pipelining process.
   d. Write the difference between serial & parallel communication.
   e. Perform the following operation on signed numbers using 2's compliment method: $(56)_{10} + (-27)_{10}$
   f. Write speed up performance laws.
   g. Differentiate between Horizontal & Vertical microprogramming.

SECTION B

2. **Attempt any *three* of the following:** **7 x 3 = 21**
   a. What is programmable logic device? List various techniques to program PLD. Explain any one technique with example.
   b. (i) Draw the block diagram for a small Accumulator based CPU
      (ii) How floating point numbers are represented in computer, also give IEEE 754 standard 32-bit floating point number format.
   c. Draw the data path of sequential n bit binary divider. Give the non restoring division algorithm for unsigned integers. Also illustrate algorithm for unsigned integer with a suitable example.
   d. What is micro programmed control unit? Give the basic structure of micro programmed control unit. Also discuss the microinstruction format and the control unit organization for a typical micro programmed controllers using suitable diagram.
   e. What do you mean by locality of reference? Explain with suitable example.

SECTION C

3. **Attempt any *one* part of the following:** **7 x 1 = 7**
   (a) Differentiate between RISC & CISC based microprocessor.
   (b) Explain Booths multiplication algorithm in detail.
4. **Attempt any *one* part of the following:** **7 x 1 = 7**
   (a) Draw the Data path of 2's compliment multiplier. Give the Robertson multiplication algorithm for 2's compliment fractions. Also illustrate the algorithm for 2's compliment fraction by a suitable example.
   (b) Describe Sequential Arithmetic & Logic unit (ALU) using proper diagram
5. **Attempt any *one* part of the following:** **7 x 1 = 7**
   (a) Give the structure of commercial 8MX 8 bit DRAM chip.
   (b) Explain the working of DMA controller with help of suitable diagrams.

Printed Pages : 2 Roll No. | | | | | | | | | | CS401

B.TECH.

THEORY EXAMINATION (SEM–IV) 2016-17

COMPUTER ORGANIZATION

Time : 3 Hours *Max. Marks : 100*

Note : Be precise in your answer. In case of numerical problem assume data wherever not provided.

SECTION-A

1 Explain the following : (10×2=20)

a) What is multiplexer? Give some applications of multiplexer.
b) Show the bit configuration of 24 bit register when its contents represent the decimal equivalent of 195 in BCD.
c) Discuss self complementing BCD code.
d) What is micro code? Explain.
e) What do you understand by wide branch addressing? Explain.
f) Write short note on RISC.
g) Write short note on indirect addressing.
h) Discuss write back method.
i) What is flash memory?
j) What is asynchronous data transfer? Explain.

SECTION-B

2 Attempt any five of the following : (10×5=50)

a) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro operation to be performed in order to change the value in A to
   i. 01101101
   ii. 11111101
b) Give the hardware implementation of following operations;-
   i. Selective set
   ii. Selective complement
c) Write a program to evaluate the arithmetic statement

   X=(A-B+C*(D*E-F))/(G+H*K)

   i. Using a general register computer with three address instructions.
   ii. Using an accumulator type computer with one address instruction.
d) Give the brief description of various I/O bus architecture.
e) What do you understand by hardwired control? Also discuss DMA.
f) Write short nots on
   i. Serial communication
   ii. Input Output Processor
g) A virtual memory has page size of 1 K words. There are 8 pages and 4 blocks. The associative memory page table contains the following entries

Page	Block
0	3

1	1
4	2
6	0

Make a list of all virtual addresses (in decimal) that will cause a page fault if used by the CPU.

h) Explain decoder. Draw the block diagram of 2 to 4 line decoder with NAND gate. Also show its truth table.

SECTION-C

Attempt any two of the following : (15×2=30)

3. Attempt the following

a) Give the block diagram of DMA controller. Why are the read and write control lines in a DMA controller bidirectional?

b) Discuss the working principle of I/O processor

4. Attempt the following

a. What do you mean by asynchronous data transfer? Explain strob controller and hand shaking mechanism for asynchronous data transfer.

b. Convert the followings

i. $(100100)_2$ = $(?)_{10}$

ii. $(235.41)_7$ = $(?)_{13}$

5. Attempt the following

a. An encoded microinstruction format is to be used. Show how a 9 bit micro operation field can be divided in to sub field to specify 46 different actions.

b. How a processor executed instructions? Define the internal functional units of a processor and how they are interconnected?

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In Pursuit of Excellence	**Question Bank**	SESSION-2019-2020
		SEM- 3rd

KCS302: Computer Organization & Architecture

[CO- 1]

1. Explain: Serial Bus Arbitration or Parallel Bus Arbitration.
2. Define Bus system? Explain the architecture of Bus system.
3. Draw a diagram for Bus System with Multiplexers or Using Tri-state Buffers.
4. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.
   d. How many selection inputs are there in each multiplexer?
   e. What size of multiplexers are needed?
   f. How many multiplexers are there in the bus?
5. Represent the following conditional control statement by two register transfer statements with control functions
   If (P = 1) then (R1 ← R2) else if (Q = 1) then R1 ← R3)
6. Consider the following register transfer statements for two 4-bit registers R1 and R2.
   xT: R1← R1 + R2
   x'T : R1 ← R2
   Draw a diagram showing hardware implementation of two statements.
7. Design an Arithmetic circuit with one variable S and two n bit data inputs A and B. The circuits generate the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages

S	C_{in} =0	C_{in} =1
0	$D = A + B$	$D = A + 1$
1	$D = A - 1$	$D = A + \bar{B} + 1$

8. Specify the Control word that must be applied to the processor to implement the following micro-operation
   f. *R1 ← R2+R3*
   g. *R4 ← R4*
   h. *R5 ← R5 – 1*
   i. *R6 ← shl R1*
   j. *R7 ← input*
9. What is stack organization? Compare register stack and memory stack.
10. Let SP =**000000** in the stack. How many items are there in the stack if:
    c. FULL = 1 and EMPTY = 0
    d. FULL = 0 and EMPTY = 1
11. Convert the following arithmetic expressions from infix to reverse polish notation.
    a. $A * B + C * D + E * F$

b. $A + B * [C * D + E * (F + G)]$

12. Convert the following arithmetic expressions from reverse Polish notation to infix notation.
    c. $ABCDE +* -/$
    d. $ABC */D - EF/+$

[CO- 2]

13. Describe carry-look ahead adder with block diagram.
14. Add -35 and -31 in binary using 8 bit registers in signed 1's complement and signed 2's complement.
15. Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation.
16. Draw the hardware details for the Booth's Multiplication algorithm and using Booth's multiplication multiply decimal numbers (-23) and (+9).
17. Perform the division process of 00001111 by 0011(use a dividend of 8 bits).
18. How floating-point numbers are represented in computer, also give IEEE 754 standard 32-bit floating point number format
19. Represent (-307.1875)10 in single precision and double precision format.

[CO- 3]

20. Write a program to evaluate arithmetic expression X= (A-B) * (((C-D * E) /F)*G)
    v. Using a general register computer with three address instructions.
    vi. Using a general register computer with two address instructions.
    vii. Using a general register computer with one address instructions.
    viii. Using a general register computer with zero address instructions.
21. A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.
    (vii) How many bits are there in the operation code, the register code part and the address part?
    (viii) Draw the instruction word format and indicate the number of bits in each part.
    (ix) How many bits are there in the data and address inputs of the memory?
22. Explain the following addressing modes with an example each:
    viii. Direct
    ix. Register Indirect
    x. Implied
    xi. Immediate
    xii. Indexed
    xiii. Relative
    xiv. Indirect
23. An instruction is stored at location 300 with its address fields at location 301. The address field has the value 400. A processor register RI contain the number 200.

Evaluate the effective address if the addressing mode of the instruction is (a) Direct (b) Immediate (c) Relative (d) Register Indirect (e) Index with RI as the Index register.

24. How a processor executed instructions? Define the internal functional units of a processor and how they are interconnected?
25. Explain all the phases of instruction cycle.
26. Write the steps in fetching a word from memory. Differentiate between branch instruction and call subroutine instruction.
27. Explain the basic concept of Hardwired and Software control unit with neat diagrams. What are the advantages and disadvantages in each control?
28. What is a microprogram sequencer? With block diagram, explain the working of microprogram sequencer.
29. What are the difference between Horizontal and vertical micro codes?

30. Differentiate between RISC & CISC based microprocessor.
31. Write short notes on:
    iv. Pipelining
    v. Indirect addressing.
    vi. Parallelism in microinstructions

[CO- 4]

32. Write the difference between RAM & ROM.
33. Explain memory hierarchy with diagram.
34. A) How many 128 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
    B) How many lines of address bus must be used to access 2048 bytes of memory. How many of these lines will be common to all chips.
    C) How many lines must be decoded for the chip select ? Specify the size of the decoder.
35. A 8-bit computer has 16-bit address bus, the first 15 lines of the address are used to select a bank of 32k bytes of memory, the higher order bit of the address is used to select a register which receives the contents of the data bus. Explain how this configuration can be used to extend the memory capacity of the system to eight banks of 32K bytes each, for a total of 256K bytes of memory.
36. A computer employs RAM chips of 256 × 8 and ROM chips of 1024 × 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for interface registers.
    iv. How many RAM and ROM chips are needed?
    v. Draw a memory-address map for the system.
    vi. Give the address ranges in hex for RAM, ROM and interface.
37. What is the transfer rate of an 8 track magnetic tape whose speed is 120 inches per second, whose density is 1600 bits per inch.
38. Consider a disk pack with the following specifications- 16 surfaces, 128 tracks per surface, 256 sectors per track and 512 bytes per sector.
    v. What is the capacity of disk pack?
    vi. What is the number of bits required to address the sector?
    vii. If the disk is rotating at 3600 RPM, what is the data transfer rate?
    viii. If the disk system has rotational speed of 3000 RPM, what is the average access time with a seek time of 11.5 msec?
39. A moving arm disc storage device has the following specifications:
    Number of Tracks per recording surface: 200
    Disc rotation speed: 2400 revolution/minute
    Track-storage capacity: 62500 bits
    Estimate the average latency and data transfer rate of this device.
40. Discuss the various types of address mapping used in cache memory.
41. What is associative memory? Explain with the help of a block diagram. Also mention the situation in which associative memory can be effective utilized.
42. A two-way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from memory. The main memory size is 128K X 32.
    v. Formulate all pertinent information required to construct the cache memory.
    vi. What is the size of cache memory?
43. A digital computer has a memory unit of 64K X 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.
    iv. How many bits are there in the tag, index, block, and words fields of the address format?
    v. How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.
    vi. How many blocks can cache accommodate?

44. Consider a cache uses a direct mapping scheme. The size of main memory is 4K byte and word size of a cache is 2 bytes. The size of cache memory is 128 bytes.
    Find the following:
    v. The size of main memory address (assume each byte of main memory has an address).
    vi. Address of a cache block.
    vii. How many memory location address will be translated to cache address/block/location?
    viii. How can it be determined if the content of specified memory address exists in cache.

[CO- 5]

45. What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each?
46. What do you mean by asynchronous data transfer? Explain strobe controller and hand shaking mechanism for asynchronous data transfer.
47. Describe in detail about programmed Input/output with neat diagram.
48. Differentiate between vectored interrupt and nonvectored Interrupt.
49. Explain the working of DMA controller with help of suitable diagrams.
50. Write short note on Input Output Processor.

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In Pursuit of Excellence	**Final Internal Marks**	SESSION-2019-2020
		SEM- 3rd

KCS302: Computer Organization & Architecture

Section A

Sno	Student Name	Roll No	CT1(15)	CT2(15)	CT3(15)	CT(30)	TA(10)	AT(10)	Total(50)
1	AASHISH PAL	1808210001	4.75	7	8	15	8	10	33
2	ABHAY VARSHNEY	1808210002	11.25	13	11.25	25	8	10	43
3	ABHAY PRATAP SINGH	1808210003	6.5	6	10.5	17	8	10	35
4	ABHISHEK	1808210005	5.5	3.25	7.75	14	8	10	32
5	ABHISHEK KUMAR	1808210006	A	3.25	9.5	13	9	8	30
6	ABHISHEK SHARMA	1808210007	A	13.25	9.75	23	8	10	41
7	ACHAL GUPTA	1808210009	6.75	8.5	9	18	8	10	36
8	ADARSH UPADHYAY	1808210010	4.5	8.5	7.25	16	8	8	32
9	AHAD NUSRAT	1808210011	A	5	7	12	10	8	30
10	AKASH BHATNAGAR	1808210013	A	12.5	10.25	23	8	9	40
11	AKASH JAUHARI	1808210014	5.5	A	10	16	4	10	30
12	AKASH KUMAR	1808210015	8.25	8	12.5	21	9	10	40
13	AKHIL KUMAR	1808210016	7.5	3.5	A	11	10	9	30
14	AKSHITA VERMA	1808210017	6.25	9	7	16	9	10	35
15	AMAN KUMAR	1808210018	7.25	4.5	A	12	10	8	30
16	AMAN VAISH	1808210019	4.25	6	A	11	9	10	30
17	AMBIKA MALHOTRA	1808210020	10	12.75	12.5	26	9	10	45
18	AMIR	1808210021	6.25	1.75	5.75	12	10	8	30
19	AMOL JAIN	1808210022	A	6.75	4.75	12	10	8	30
20	ANIKET SINGH	1808210025	7.25	3.25	A	11	10	9	30
21	ANIL KUMAR	1808210026	4.25	6.5	A	11	10	9	30
22	ANIL KUMAR	1808210027	4.5	0.5	5.5	10	10	10	30
23	ANKIT CHANDRA	1808210028	5	2.5	7	12	10	8	30
24	ANKIT KUMAR	1808210029	3.25	3.75	8	12	10	8	30
25	ANKUSH TYAGI	1808210030	4	4.75	9.75	15	9	9	33
26	ANSHDEEP TYAGI	1808210031	A	4	8	12	10	8	30
27	ANSHIKA GOEL	1808210032	A	6.75	9	16	9	10	35
28	ANUBHAV MISHRA	1808210033	3.75	7	4	11	10	9	30
29	ANUBHAV SHUKLA	1808210034	4.5	7	2.25	12	10	8	30
30	ASEEM GUPTA	1808210036	5.5	5	10.5	16	10	10	36
31	AVNISH KUMAR	1808210037	1.75	7.75	7.5	16	8	8	32
32	AYUSH KUMAR SINGH	1808210038	5	0.5	7	12	10	8	30

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33	AYUSH SHARMA	1808210039	7.75	10	3.5	18	8	10		36
34	BHASKAR SAINI	1808210040	5.5	1.5	6	12	10	8		30
35	BHUVNESH KUMAR SHARMA	1808210041	5.25	12	13	25	10	10		45
36	BILAL SAIFI	1808210042	4.5	4.5	9.5	14	8	8		30
37	BOBI KHAN	1808210043	A	A	10	10	10	8		28
38	CHANDR VEER SINGH	1808210044	5	4.5	7	12	10	8		30
39	DEEKSHA SINGH	1808210046	4.75	A	9	14	7	9		30
40	DEEPENDRA SINGH RAGHAV	1808210047	7.5	A	8.25	16	6	8		30
41	DEVAL JHINGRAN	1808210048	10.75	7.25	10	21	9	9		39
42	DEVESH BHARDWAJ	1808210050	7.25	11.5	11	23	9	10		42
43	GAGAN	1808210051	1.75	2.5	10.25	13	8	9		30
44	GARVIT BHOLA	1808210052	5.25	12.5	11.25	24	9	9		42
45	GAURANG GUPTA	1808210053	3.25	2	9.5	13	9	8		30
46	GAURANGEE BHARDWAJ	1808210054	8.25	12.25	13.25	26	9	10		45
47	GAURAV BHATNAGAR	1808210055	A	5.25	7	13	9	8		30
48	GAURAV KUMAR	1808210056	2	6	5.75	12	10	8		30
49	GEETIKA GUPTA	1808210057	10.5	11	9	22	10	10		42
50	HAMMAD HUSSAIN	1808210058	4.25	2.5	6.5	11	10	9		30
51	HARSH GUPTA	1808210059	8	13	12.5	26	9	10		45
52	HARSH VARDHAN	1808210060	A	8.5	8.75	18	9	9		36
53	HARSHBEER SINGH	1808210061	14.5	14.75	A	30	10	9		49
54	HARSHIT KUMAR	1808210062	A	2.5	9	12	10	8		30
55	HARSHIT PANDEY	1808210063	A	8	5.5	14	9	9		32
56	HONEY TYAGI	1808210064	3.5	12.5	A	16	5	9		30
57	IRAM RAFI	1808210066	10	8.5	A	19	8	9		36
58	ISHAN SAXENA	1808210067	5	10	4.5	15	9	10		34

Section C

Sno	Student Name	Roll No	CT1(15)	CT2(15)	CT3(15)	Makeup	CT(30)	TA(10)	AT(10)	Total(50)
1	SANKALP GUPTA	1808210131	4.25	6	9.5	A	16	10	10	36
2	SANSKRITI AGARWAL	1808210132	10.5	12.5	5.5	A	23	8	8	39
3	SARTHAK SAXENA	1808210133	5.25	A	6.25	A	12	10	8	30
4	SATAKSHI	1808210134	6	5.75	A	A	12	10	8	30
5	SAURABH KUMAR	1808210135	6.5	8.75	9	A	18	10	10	38
6	SAYYDUL MILLAT	1808210136	A	3	9	3	12	10	8	30
7	SHAZAR ZAIDI	1808210137	3.25	1.5	8.25	A	12	9	9	30
8	SHIVANI TYAGI	1808210138	A	5.25	6.5	A	12	10	8	30
9	SHIVANSH MATHUR	1808210139	9.5	7.5	10	A	20	9	8	37
10	SHIVANSH AGARWAL	1808210140	5.25	11	10	A	21	10	10	41
11	SHIVANSHU AGARWAL	1808210141	4	5.25	6.75	6.75	12	10	8	30
12	SHREY RUHELA	1808210142	2.25	3.5	7.25	A	11	10	9	30
13	SHREYA CHAUHAN	1808210143	4.5	2	7.5	A	12	10	8	30
14	SHUBH BHATNAGAR	1808210144	5	A	8.75	A	14	10	8	32
15	SHUBHAM YADAV	1808210146	6	5.75	8.5	A	15	6	9	30

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16	SHUBHIKA SINGH	1808210147	5.25	3.5	8.5	A	14	8	8	30
17	SOURABH SAINI	1808210148	5.75	3.25	5	5	11	10	9	30
18	SPARSH RASTOGI	1808210149	4.5	7.5	A	A	12	10	8	30
19	SRIJAN PANDEY	1808210150	3.75	A	8.25	A	12	10	8	30
20	SUFIYA	1808210151	11.5	12.75	12	A	25	9	8	42
21	SUHAIL AHMED	1808210152	A	3	8.75	3	12	10	8	30
22	SUKRITI SINGH	1808210153	7.75	1.25	7	A	15	7	8	30
23	SUMIT KUMAR	1808210154	3.5	8	7.75	A	16	8	9	33
24	SUSHANT KUMAR	1808210155	6	5	5.5	A	12	9	9	30
25	SUSHANT SINGH	1808210156	A	5	9	A	14	8	8	30
26	TANVEER ALAM	1808210157	6	4.5	5.25	A	12	9	9	30
27	UDIT RAJPUT	1808210158	9	12.5	13	A	26	9	9	44
28	UMANG MATHUR	1808210159	4.5	6.25	A	A	11	10	9	30
29	UNNATI GANGWAR	1808210160	6.25	1	5.25	A	12	10	8	30
30	UNNATI SINGH	1808210161	4.25	2.75	6.25	A	11	10	9	30
31	UTKARSH GUPTA	1808210162	7.5	4	A	A	12	10	8	30
32	VASU GOEL	1808210164	8	A	4	4	12	10	8	30
33	VASUNDHRA GUPTA	1808210165	6.75	1.5	7.5	A	15	9	8	32
34	VEDIKA AGARWAL	1808210166	6.75	1	5	A	12	10	8	30
35	VINAYAK VARSHNEY	1808210167	9	6.75	7.75	A	17	8	10	35
36	VIRENDRA MOHAN	1808210168	5.5	0.25	6.25	A	12	10	8	30
37	VISHAL TYAGI	1808210170	5	A	7.75	A	13	9	8	30
38	YASH AGARWAL	1808210171	5.5	6	8.5	A	15	6	9	30
39	ZAMAN ABBAS	1808210172	A	7.75	4.25	7.75	12	10	8	30
40	ANUJ SHARMA		5	4	7	A	12	10	8	30
41	UDIT		5.25	0	6.25	A	12	10	8	30
42	SATYAM RASTOGI		5.25	2	4.75	A	10	10	10	30
43	ZAREEN AQIQ		5	A	7	A	12	10	8	30
44	VISHAL SAINI		6.25	2.75	7.5	A	14	8	8	30
45	HADIYA KHALEEQ		4.25	5.25	9	A	15	9	8	32

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In Pursuit of Excellence	Course outcome Attainment	SESSION-2019-2020
		SEM- 3rd

KCS302: Computer Organization & Architecture

CO Attainment and Analysis

Direct CO Attainment using Continuous Internal Examination (CIE)

Course Code	CO	CO Attained (% of students getting ≥ 60% marks)	CO Attained (On Scale of 3)
KCS302	CO1	89.32	2.68
	CO2	77.67	2.33
	CO3	96.12	2.88
	CO4	95.15	2.85
	CO5	76.7	2.3

Direct CO Attainment using Semester End Examination (SEE)

Course Code	CO	CO Attained (% of students getting ≥ 60% marks)	CO Attained (On Scale of 3)
KCS302	CO1	19.42	0.58
	CO2	19.42	0.58
	CO3	19.42	0.58
	CO4	19.42	0.58
	CO5	19.42	0.58

Direct CO Attainment (CO_Direct)

Course Code	CO	CO Attained Using CIE (CO_CIE)	CO Attained using SEE (CO_SEE)	Direct CO Attainment (CO_Direct = 0.33*CO_CIE + 0.67*CO_SEE)	Direct CO Attainment (On Scale of 3)
KCS302	CO1	89.32	19.42	42.49	1.27
	CO2	77.67	19.42	38.64	1.16
	CO3	96.12	19.42	44.73	1.34
	CO4	95.15	19.42	44.41	1.33
	CO5	76.7	19.42	38.32	1.15

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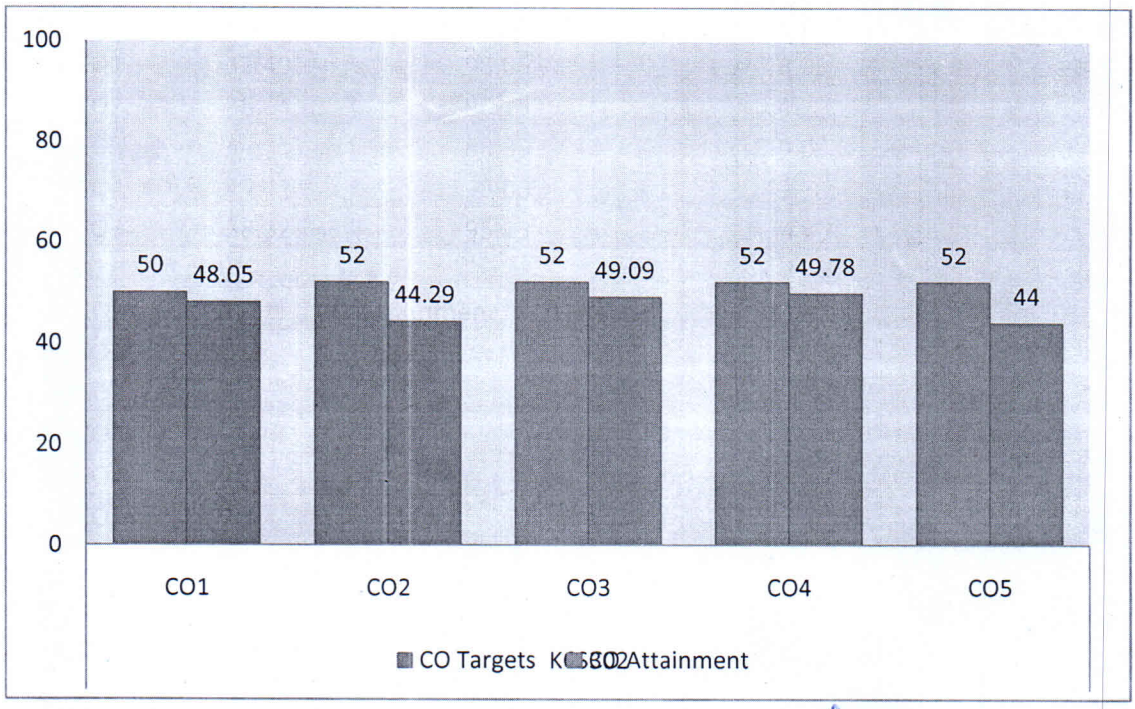
Indirect CO Attainment (CO_Indirect)

Course Code	CO	Indirect CO Attainment (CO_Indirect)	Indirect CO Attainment (On scale of 3)
KCS302	CO1	98.06	2.94
	CO2	95.15	2.85
	CO3	88.35	2.65
	CO4	98.06	2.94
	CO5	95.15	2.85

CO Attainment

Course Code	CO	Direct CO Attainment (CO_Direct)	Indirect CO Attainment (CO_Indirect)	CO Attainment (CO = 0.9*CO_Direct + 0.1*CO_Indirect)	CO Attainment (On scale of 3)	Y/N
KCS302	CO1	42.49	98.06	48.05	1.44	N
	CO2	38.64	95.15	44.29	1.33	N
	CO3	44.73	88.35	49.09	1.47	N
	CO4	44.41	98.06	49.78	1.49	N
	CO5	38.32	95.15	44	1.32	N

Course Code	CO	CO Targets	CO Attainment	Y/N
KCS302	CO1	50	48.05	N
	CO2	52	44.29	N
	CO3	52	49.09	N
	CO4	52	49.78	N
	CO5	52	44	N



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Closure of Quality Loop

Course Code	CO	CO Targets	CO Attainment Gap	Action proposed to bridge the gap where targets are not achieved	Modification of targets where Achieved
KCS302	CO1	50	1.95	More examples on Register Transfer, Adressing modes will be covered.	
	CO2	52	7.71	More focus will be on providing the understanding of arithmetic algorithms	
	CO3	52	2.91	Short note on microprogrammmed control will be provided.	
	CO4	52	2.22	Examples will be added on cache memory and virtual memory.	
	CO5	52	8.00	Short note on IOP and DMA will be provided	

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KCS 302
L T P
3 1 0

KCS 352
L T P
0 0 2

KCS 302

Computer Organization & Architecture

KCS 302
Evaluation Scheme

CT	TA	Internal
30	20	50

Best 2 out of 3

External
100

KCS352

Internal	External
25	25

Objectives

This course is all about

→ How computer "works"

→ to know performance needs

- Algorithm determine no of statement
- Language / Compiler / Architecture determine machine instructions
- Processor / Memory determine how fast instructions are executed
- I/O and no of cores determine overall system performance

Text books

1. Computer System Architecture – M. Mano
2. Computer Organisation – Carl Hamacher, Zvonko Vranesic Safwat Zaky.
3. Computer Architecture – A Quantative Approach – David A. Patterson and John L. Hennessy.

Computer Organization

↳ is concerned with the way the hardware components are connected together to form a computer system.

Computer Architecture

↳ is concerned with the structure and behaviour of the various functional modules/unit of the computer and how they interacted to provide the processing needs of the user.

First Generation

1946 - 1959 ENIAC

Second

1959 - 1965

Third

1965 - 1971

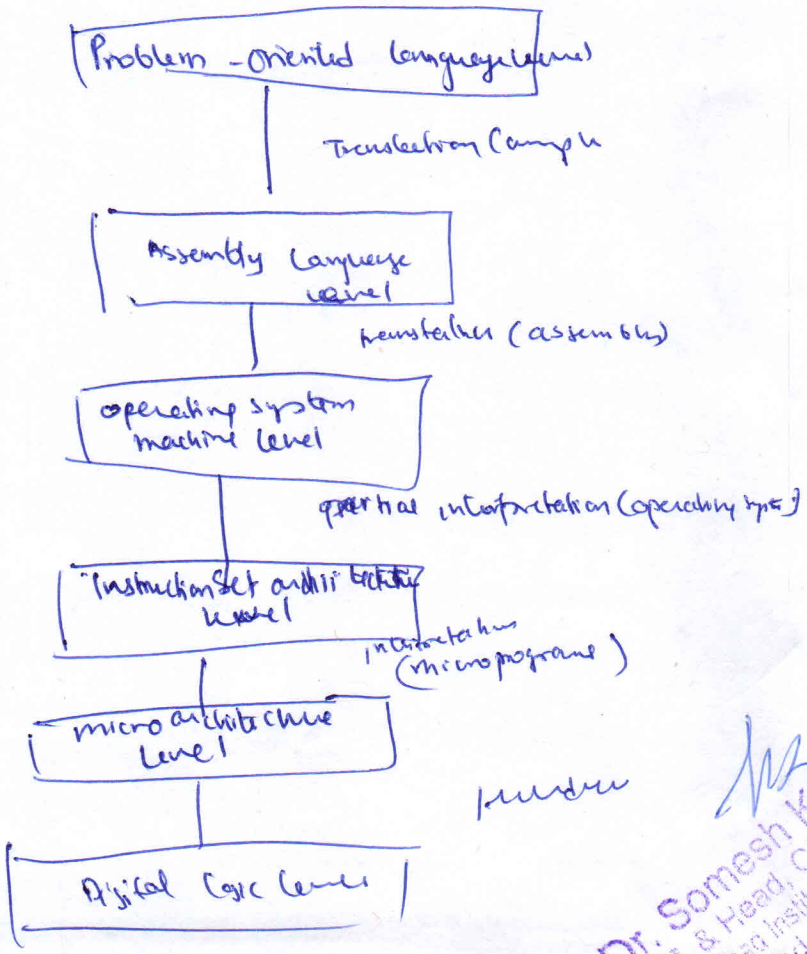
fourth

1971 - 1980 - micro processor

fifth

1980 - ——— Ultra large scale Integration

AI



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Bus Arbitration

Bus Master: The device that is allowed to initiate data transfers on the bus at any given time is called the bus master

When the current master relinquishes control of the bus, another device can acquire this status.

Bus Arbitration is the process by which the next device to become the bus master is selected and bus mastership is transfered to it.

The selection of the bus master must take into account the needs of various devices by establishing a priority system for gaining access to the bus.

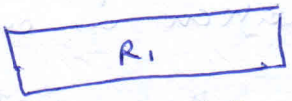
Serial Arbitration / Daisy-chain Arbitration / Centralized Arbitration

In serial bus Arbitration, The devices/arbiters are connected serially to the system bus are assigned priority according to their position along the priority line.

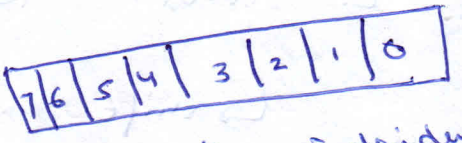
* Each Arbiter has Priority-in (PI) and Priority-out (PO) lines
* The priority out (PO) of each arbiter is connected to the priority in (PI) of next lower priority arbiter.

Register Transfer and Microoperation

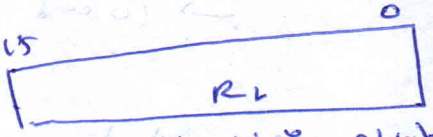
Register



a) Register R_1



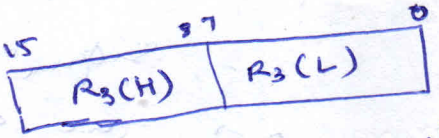
b) showing individual bits



Numbering of bits

c)

d)



Divided in part

Representation of Register

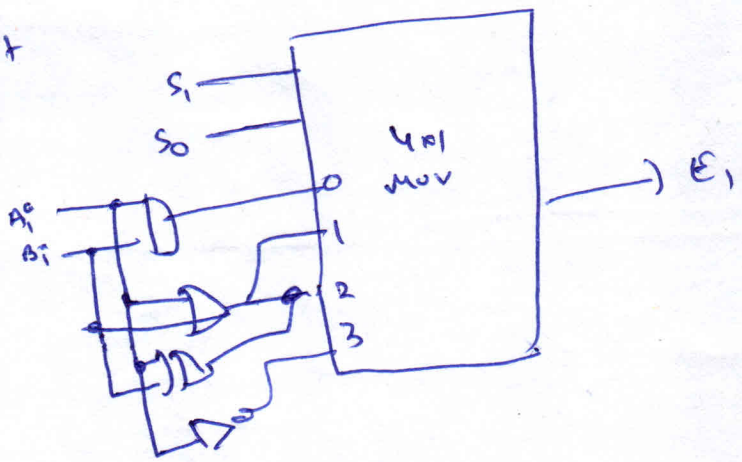
Basic symbols		
Letters (and Numerals)	Denote a register	MAR, R_2
Parenthesis ( )	Denote a part of Register	$R_2(0-7)$, $R_2(L)$
Arrow ←	Denotes the transfer of information	$R_2 \leftarrow R_1$
Comma ,	Separate two microoperations	$R_2 \leftarrow R_1$, $R_1 \leftarrow R_2$

Logic Micro operations specify binary operations on bits stored in register

$P: R1 \leftarrow R_1 \oplus R_2$

```
1010    Content of R1
1100    Content of R2
----
0110    Contents of R1 after P=1
```

Logic unit



S1 S0	output	
0 0	$E = A \wedge B$	AND
0 1	$E = A \vee B$	OR
1 0	$E = A \oplus B$	XOR
1 1	$E = \bar{A}$	Complement

Selective - Set

The selective-set operation sets to 1 the bits in register A where there are corresponding 1's in register B.

```
1010     A before
1100     B (logic operation)
----
1110     A after
```

OR Microoperation is used

Selective complement ~~operation~~

The selective-complement operation complements bits in A where there are corresponding 1's in B.

```
1010     A before
1100     B
----
0110     A after
```

X-OR Microoperation is used

Selective-clear

Selective clear operation clears to 0 the bits in A only where there are corresponding 1's in B

```
1010     A before
1100     B
----
0010     A after
```

$A \leftarrow A \wedge \bar{B}$ microoperation is used

Mask operation

is similar to the selective-clear operation except that the bits of A are cleared only where there are corresponding 1's in B

AND Micro operation in use

```
1010    A before
1100    B
----
1000    A after masking
```

Insert operation

inserts a new value into a groups of bits. This is done by first masking the bits and then ORing them with the required bits

~~Old~~. Suppose A has 0110 1010, ~~Need~~ to replace ~~bits from~~ first four bits with 1001

Mask [AND]

```
0110  1010    A before
0000  1111    B (mask)
---------
0000  1010    A after masking
```

Insert [OR]

```
0000  1010    A before
1001  0000    B (insert)
---------
1001  1010
---------
```

Clear — operation compares words in A and B and produce an all 0's result if the two number are equal

```
1010      A
1010      B
----------
0000      A ← A ⊕ B
```