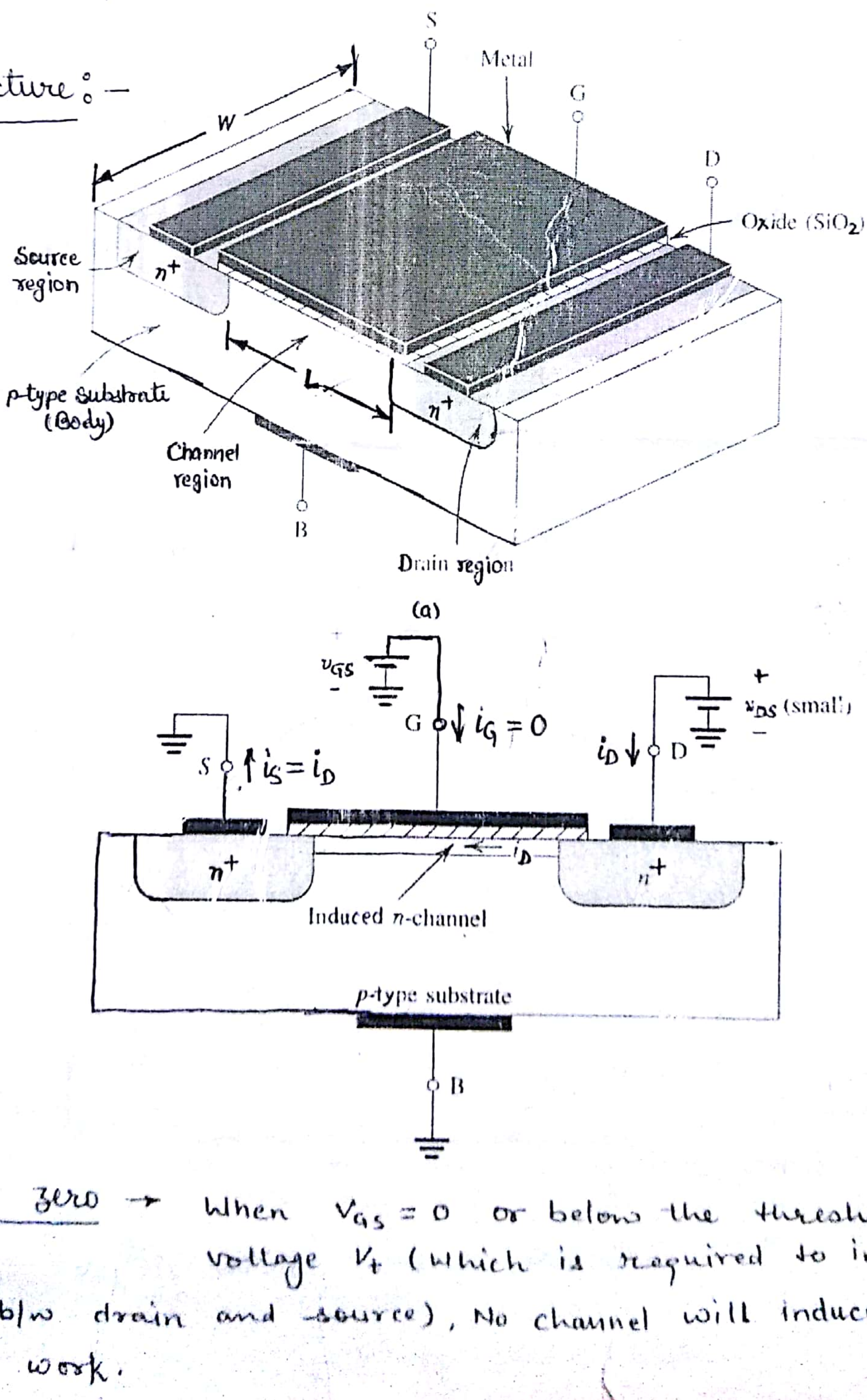
MOSFET :- [Metal Oxide Semiconductor Field Effect Transistor]

* MOSFET can be made quite small than BJT. [requiring small area on silicon IC chip]
* Relative simple manufacturing process.
* Requirement of comparatively little power.
* Implementations of analog and digital f^n's with very few or no resistors is possible with MOSFET.

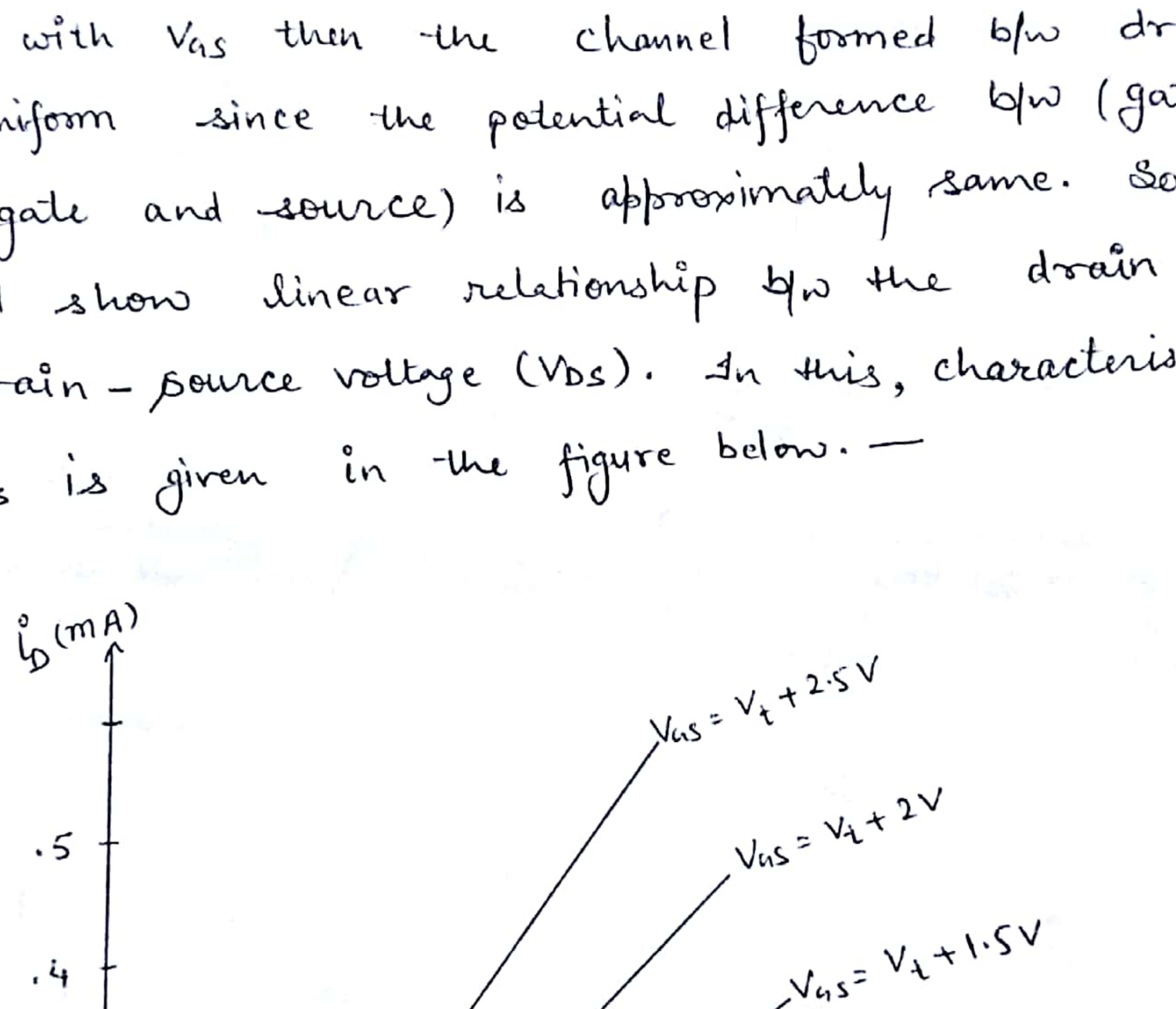
Device Structure :-



(i)- When V_{GS} is zero → When $V_{GS} = 0$ or below the threshold voltage V_t (which is required to induce the channel b/w drain and source), No channel will induce and device won't work.

(ii)- Some positive voltage ($V_{GS} \geq V_t$) is applied to Gate terminal → When $V_{GS} \geq V_t$ is applied, the channel is formed b/w drain and source and now the current can flow from drain to source through this induced channel.

(iii)- When V_{DS}, applied to drain is very less (small) → When V_{DS} is as small as it can be negligible with V_{GS} then the channel formed b/w drain as source is uniform since the potential difference b/w (gate and drain) and (gate and source) is approximately same. So the MOSFET will show linear relationship b/w the drain current (i_D) and drain - source voltage (V_{DS}). In this, characteristics b/w i_D and V_{DS} is given in the figure below. —



[When V_{DS} is small] i_D-V_{DS} characteristics

(iv) Operation as V_{DS} Increased :- Let V_{GS} be held constant at a value greater than V_t.

* V_{DS} appears as the voltage drop across the length of the channel. i.e. as we move along the channel from source to drain, the voltage increases from 0 to V_{DS}.

* voltage b/w gate and the points along the channel decreases from V_{GS} at the source to $V_{GS} - V_{DS}$ at the drain terminal. Depth of the channel depends upon this voltage. So now we can conclude that the channel depth is no longer uniform. channel will take the tapered form as shown in figure (below ①) the i_D-V_{DS} characteristics)

[on the opposite page] ②

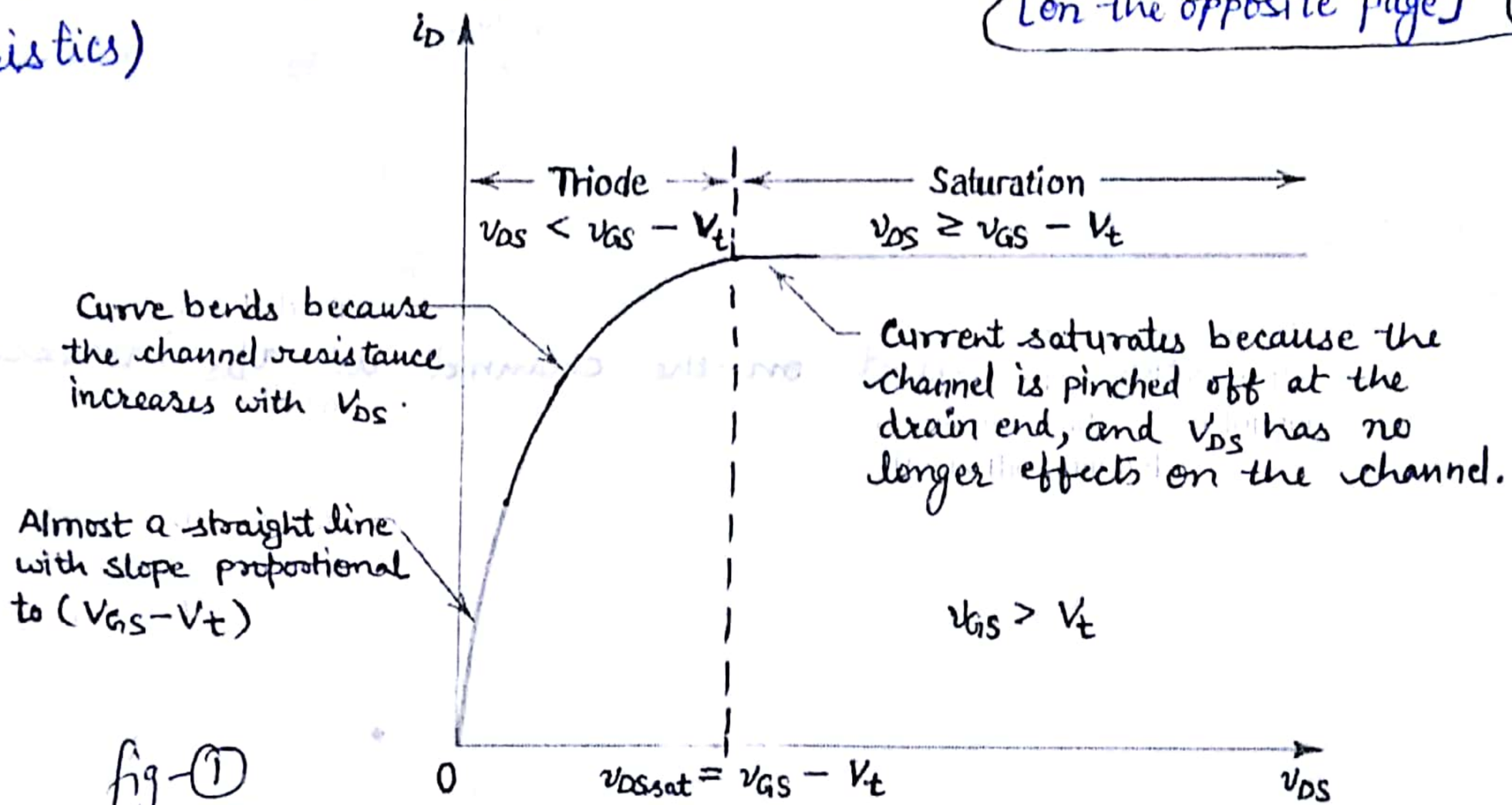


fig-①

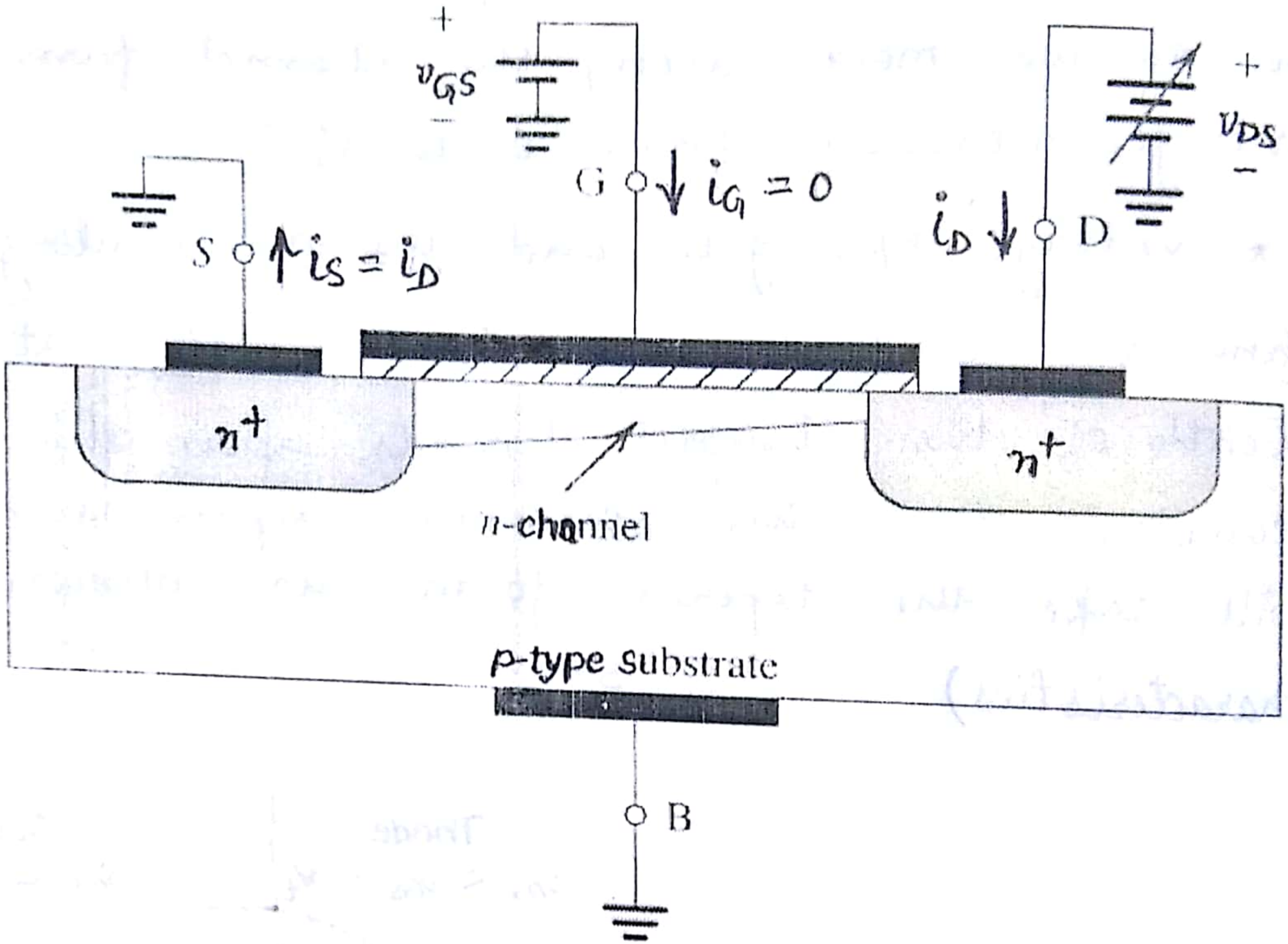


Fig ② Effect on the channel as V_{DS} increased.

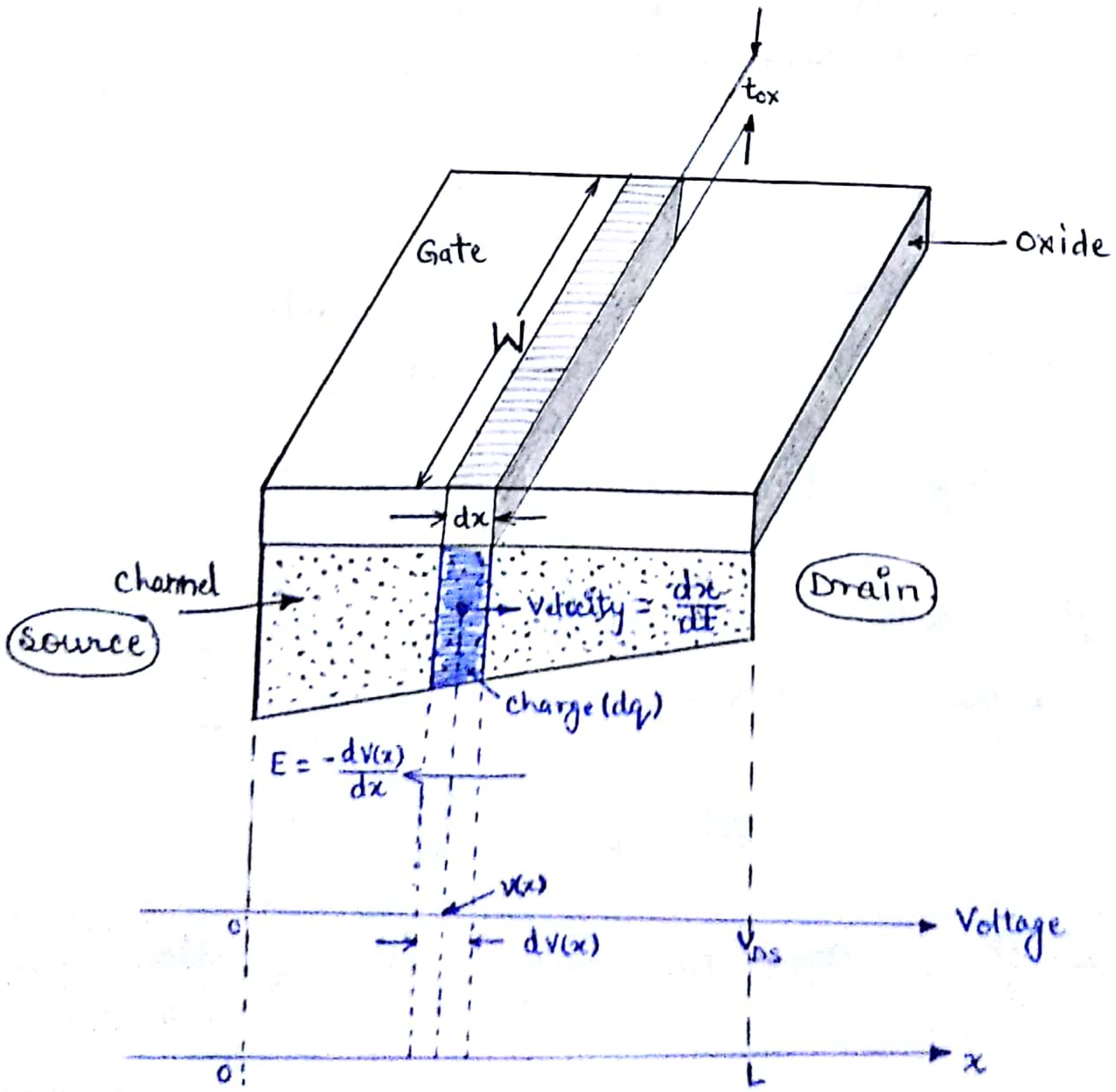
Derivation of the $i_D - V_{DS}$ Relationship :— Assume that the voltage applied to Gate terminal (V_{GS}) is greater than the threshold voltage (V_t). Also assume that a voltage V_{DS} is applied b/w drain & source.

For the Triode region the channel is continuous and the voltage $V_{DS} < V_{GS} - V_t$.

Now the Gate and channel region forms a parallel plate capacitor and the oxide layer between them is behaving like a dielectric. If the thickness of oxide layer is t_{ox} and ε_{ox} is the permittivity of SiO_2 then the capacitance per unit gate area is given by —

$$C_{ox} = \frac{\varepsilon_{ox} A}{t_{ox}} = \frac{\varepsilon_{ox}}{t_{ox}} \quad \left\{ \because A = 1 \text{ per unit gate area} \right\}$$

$$\varepsilon_{ox} = 3.9\,\varepsilon_0 = 3.45 \times 10^{-11}\ F/m \quad [\text{for } SiO_2]$$



Let us assume an infinitesimal strip of distance 'dx' of gate plates and the thickness of oxide is t_{ox}. If the length of the device is W then its capacitance is given by –

$$C_{ox} W dx .$$

To find the charge stored in this infinitesimal strip we multiply the capacitance by the effective voltage b/w gate and channel at point x. Where effective voltage stands for the voltage responsible to induce channel b/w drain & source.

At point x this voltage is equal to $[V_{GS} - V(x) - V_t]$.

where $V(x)$ is the voltage in the channel at point x.

Now the charge present in the infinitesimal portion of the channel at point x is –

$$dq_r = - C_{ox} W dx [V_{GS} - V(x) - V_t] \qquad [\because Q = CV]$$

['-' sign stands for negative charge.]

V_{DS} produces an electric field along the channel in the -ve x direction. At point x this field is given by –

$$E(x) = - \nabla V(x) = - \frac{dV(x)}{dx}$$

This electric field causes the electron charge dq_r to drift towards the drain with a velocity dx/dt.

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dV(x)}{dx} \qquad [\mu_n = \text{Mobility of } e^-s]$$

Because of the movement of charge dq_r, a current will flow in the channel from drain to source.

$$i = \frac{dq_r}{dt} = \frac{dq_r}{dx} \cdot \frac{dx}{dt}$$

$\frac{dq_r}{dx} \rightarrow$ charge per unit length ; $\frac{dx}{dt} \rightarrow$ electron drift velocity.

$$i = -\mu_n C_{ox} W \left[V_{GS} - V(x) - V_t\right] \frac{dV(x)}{dx} = -i_D \quad [\text{drain current}]$$

$$i_D = \mu_n C_{ox} W \left[V_{GS} - V(x) - V_t\right] \frac{dV(x)}{dx}$$

$$\int_0^L i_D \, dx = \int_0^{V_{DS}} \mu_n C_{ox} W \left[V_{GS} - V(x) - V_t\right] dV(x)$$

{ dx [channel length varies from 0 to L]
V(x) [channel voltage varies from 0 to V_{DS}] }

$$i_D \cdot L = \mu_n C_{ox} W \left[(V_{GS} - V_t)V_{DS} - \frac{1}{2} V_{DS}^2\right]$$

$$\boxed{i_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_t)V_{DS} - \frac{1}{2} V_{DS}^2\right]}$$

This is the general expression for $I_D - V_{DS}$ characteristics.

In triode region this expression remains unchanged. and for Saturation region substituting $V_{DS} = V_{GS} - V_t$ the expression changes (modifies) in the way as —

$$\boxed{i_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) \left[V_{GS} - V_t\right]^2}$$

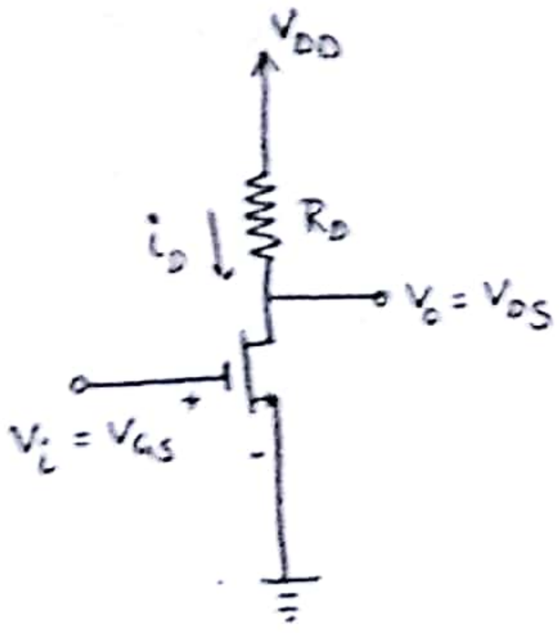
$\mu_n C_{ox}$ = Constt. depends on the process of fabrication.
↳ (k'_n) Also called Process conductance parameter.

$\frac{W}{L}$ = Aspect Ratio = $\frac{\text{channel width}}{\text{channel Length}}$.

MOSFET as an amplifier and as a switch :- When MOSFET operated in the saturation region, the MOSFET acts as a voltage-controlled current source. If V_{GS} changes i_D also changes.

Firstly we will study the large-signal operation of MOSFET amplifier by deriving the voltage transfer characteristics of a commonly used MOSFET amplifier circuit. From these characteristics we can clearly see the regions where it can be operated as a switch and can be biased to operate as small signal amplifier.

Large Signal operations :-



(i)- Common-Source Amp^r
or
Grounded Source

(ii)- Graphical construction to determine the transfer characteristics of the amplifier.

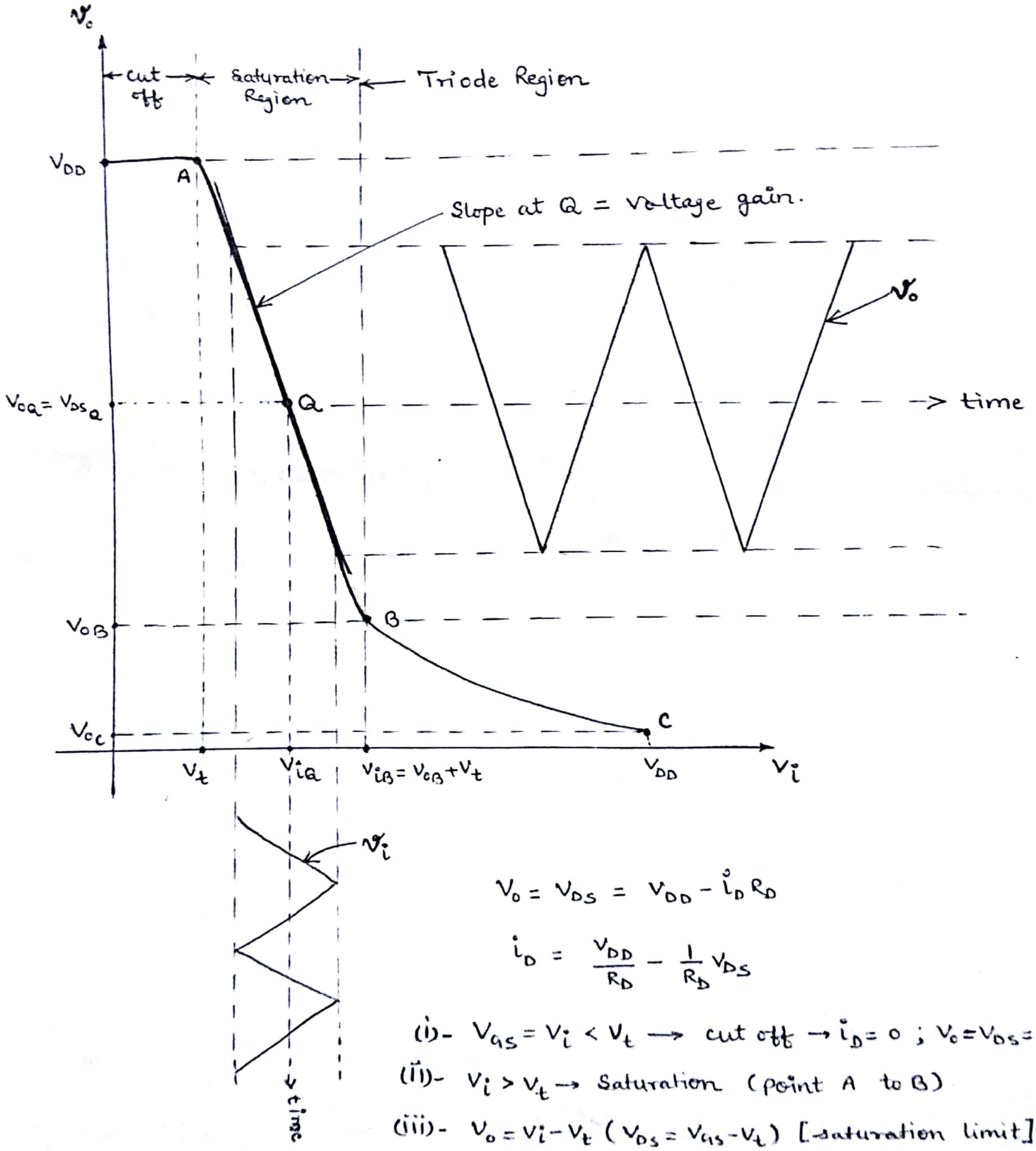
By changing the V_i or V_{GS} we can change the i_D and since we are using a resistor R_D so the o/p voltage obtained is -

$$\boxed{V_o = V_{DS} = V_{DD} - i_D R_D}$$

In this way the transconductance amplifier in converted into a voltage amplifier.

Now we need to plot the relationship between V_o & V_i. We can do this analytically and graphically. [Transfer characteristics]

Graphical Derivation of T/F characteristics :-



$$V_o = V_{DS} = V_{DD} - i_D R_D$$

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} V_{DS}$$

(i)- $V_{GS} = V_i < V_t \longrightarrow$ cut off $\rightarrow i_D = 0$; $V_o = V_{DS} = V_{DD}$

(ii)- $V_i > V_t \rightarrow$ Saturation (point A to B)

(iii)- $V_o = V_i - V_t$ ($V_{DS} = V_{GS} - V_t$) [saturation limit]

↳ Enters into triode region (point B to C)

(iv)- $V_i = V_{DD} \rightarrow V_o = V_{oC}$ (point C)

Analytical Expression for Transfer characteristics :-

1- Cut-off (segment-'XA') Region →

$$V_i < V_t$$

So $\quad v_o = V_{DD}$

2- Saturation Region (Segment-'AQB') →

$$V_i \geq V_t$$

$$v_o \geq V_i - V_t$$

$$i_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(V_i - V_t)^2$$

$$v_o = V_{DD} - i_D R_D$$

$$v_o = V_{DD} - \frac{1}{2} R_D \mu_n C_{ox} \left(\frac{W}{L}\right)(V_i - V_t)^2$$

The voltage gain A_V at the bias point Q is

$$A_V = \left.\frac{dv_o}{dV_i}\right|_{V_i = V_{IQ}}$$

$$A_V = -\frac{2}{2} R_D \mu_n C_{ox} \frac{W}{L}(V_{IQ} - V_t)$$

$$\boxed{A_V = -R_D \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{IQ} - V_t)}$$

$A_V \propto R_D$

$A_V \propto \mu_n C_{ox} \rightarrow$ Transconductance parameter

$A_V \propto \frac{W}{L} \rightarrow$ Transistor Aspect Ratio.

$A_V \propto (V_{IQ} - V_t) \rightarrow$ overdrive voltage at bias point 'Q'.

3- Triode Region (Segment - 'BC') →

$$V_i \geq V_t$$

$$v_o \leq V_i - V_t$$

$$i_D = \mu_n C_{ox} \frac{W}{L} \left[(V_i - V_t) v_o - \frac{1}{2} v_o^2 \right] \quad \{ \text{Triode Region Drain-current} \}$$

$$v_o = V_{DD} - i_D R_D$$

$$v_o = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L} \left[(V_i - V_t) v_o - \frac{1}{2} v_o^2 \right]$$

$$v_o \simeq V_{DD} - R_D \mu_n C_{ox} \frac{W}{L} (V_i - V_t) v_o \quad \{ v_{DS} = v_o \rightarrow \text{Sufficiently small} \}$$

$$v_o = \frac{V_{DD}}{\left[1 + R_D \mu_n C_{ox} \frac{W}{L} (V_i - V_t) \right]} \quad \text{——— ①}$$

$$i_D = \mu_n C_{ox} \frac{W}{L} (V_i - V_t) v_o \quad \{ \text{Sufficiently small } v_o \text{ or } V_{DS} \}$$

$$\frac{v_o}{i_D} = r_{DS} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L} \right) (V_i - V_t)}$$

Putting this value of r_{DS} in eq^n ①

$$v_o = \frac{V_{DD}}{\left(1 + \frac{R_D}{r_{DS}} \right)} \Rightarrow V_{DD} \frac{r_{DS}}{r_{DS} + R_D}$$

$$\boxed{v_o = V_{DD} \frac{r_{DS}}{r_{DS} + R_D}}$$

Biasing in MOS Amplifier circuits →

* Establishment of an appropriate dc operating point, bias point or Quiescent point is called Biasing technique.
* To identify stable and predictable drain current, V_{DS} which ensures operation in saturation region. for all expected i/p signals (v_{gs}).

1- Biasing by fixing V_{GS} →

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 \longrightarrow \text{In Saturation Region.}$$

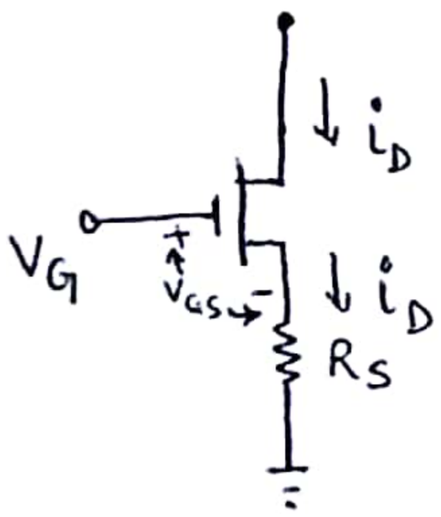
Whichever value of I_D is required we can find a suitable V_{GS} for it.

→ μ_n, C_{ox}, $\frac{W}{L}$ can have diff. values for diff- $\frac{2}{}$ devices.

→ MOSFET may be fabricated on diff. types of wafers.

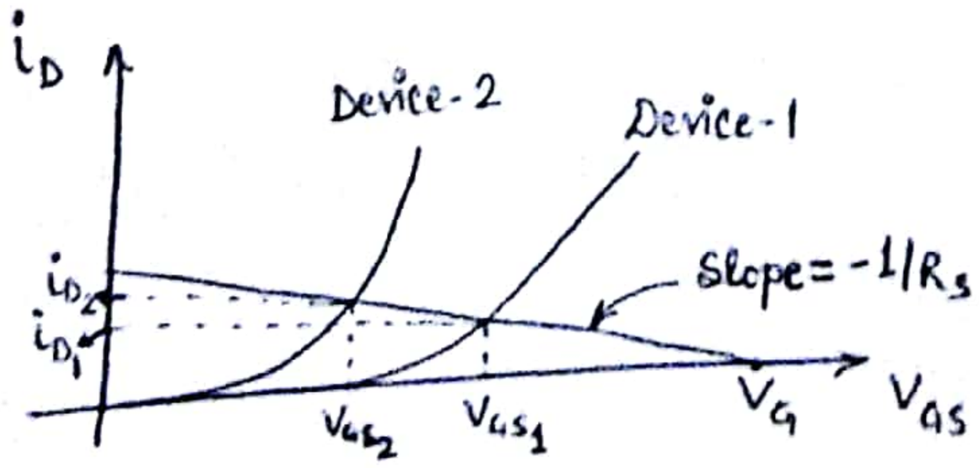
→ V_t, μ_n are temperature dependent, make I_D dependent on temperature.

2- Biasing by fixing V_G and connecting a Resistance in Source →

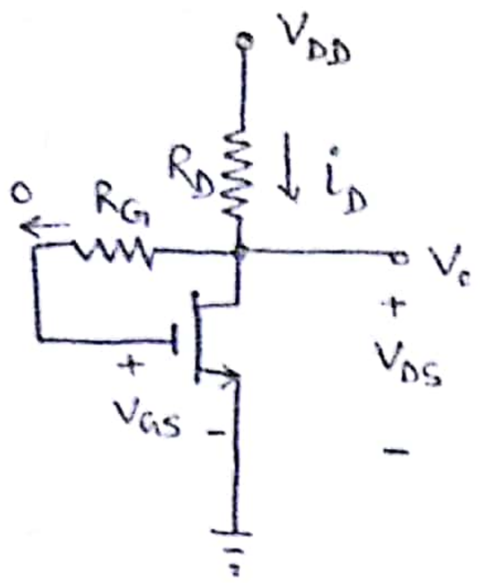


$$V_G = V_{GS} + i_D R_S$$

Suppose i_D increases due to any possible reason. V_G is constt. so V_{GS} has to decrease which inturn causes i_D to decrease. Thus the action of R_S works to keep i_D as constt. as possible. This 'Negative f/b action of R_S gives R_S the name "degeneration resistance"



3- Biasing using a Drain to Gate Feedback Resistor →



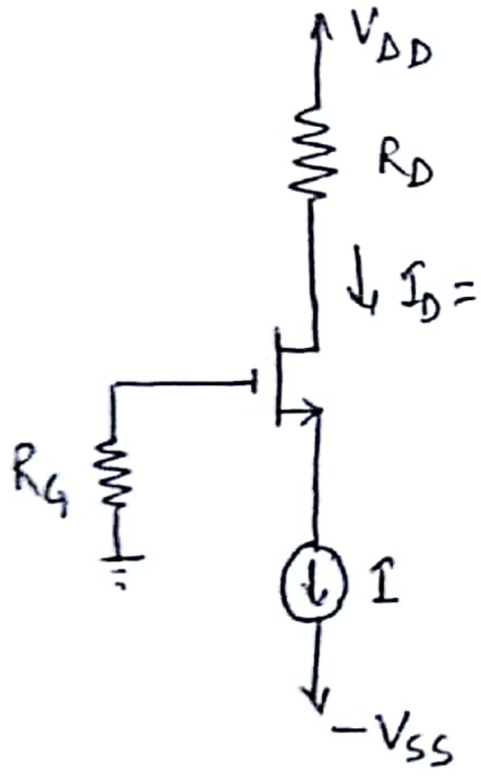
$R_G \simeq$ Mega ohms $\rightarrow$ $I_G = 0 \rightarrow V_G \simeq V_D$

$$V_{GS} = V_{DS} = V_{DD} - I_D R_D$$

$$V_{DD} = V_{GS} + I_D R_D$$

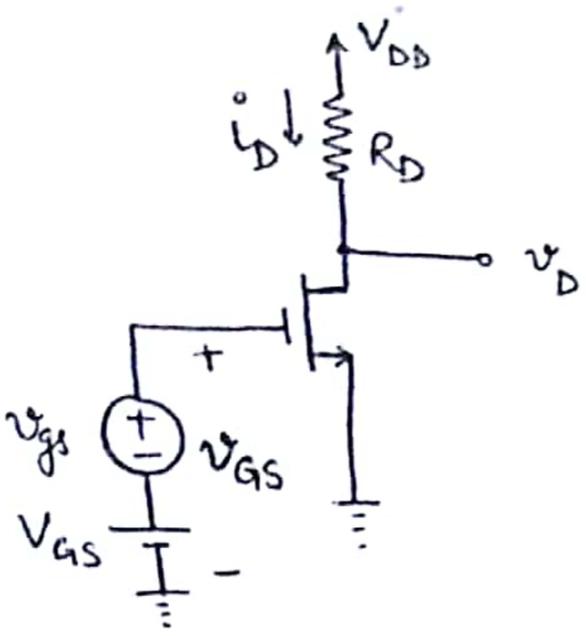
$I_D \uparrow$; V_{DD} = constt $\rightarrow$ $V_{GS} \downarrow \rightarrow I_D \downarrow$

4- Biasing using a constt. current source →



Small Signal operation and Models :-

In the previous section we learned that linear amplification can be achieved by biasing the MOSFET in saturation region and by keeping the small i/p signal.



$$v_{GS} = V_{GS} + v_{gs} \quad [\text{Total Instantaneous Gate-source voltage}]$$

$$i_D = \frac{1}{2} k_n' \frac{W}{L} \left[V_{GS} + v_{gs} - V_t \right]^2 \quad \{\text{Total Instt. drain current}\}$$

$$= \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 + k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} + \frac{1}{2} k_n' \frac{W}{L} v_{gs}^2$$

So this current is constituted by 3 types of currents. —
1st part can be recognized as dc bias current I_D. 3rd, 2nd terms represents the current components that are proportional to the square of i/p voltage v_{gs} and directly proportional to i/p voltage v_{gs} respectively.

3rd part is undesirable because it represents nonlinear distortion. to reduce this

$$\frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} \gg \frac{1}{2} k_n' \frac{W}{L} v_{gs}^2$$

$$v_{gs} \ll 2(V_{GS} - V_t)$$

$$v_{gs} \ll 2 V_{ov}$$

$V_{ov} \rightarrow$ overdrive voltage at which transistor is operating.

If this small signal condition is satisfied we may neglect the last term and can represent the same eqn as —

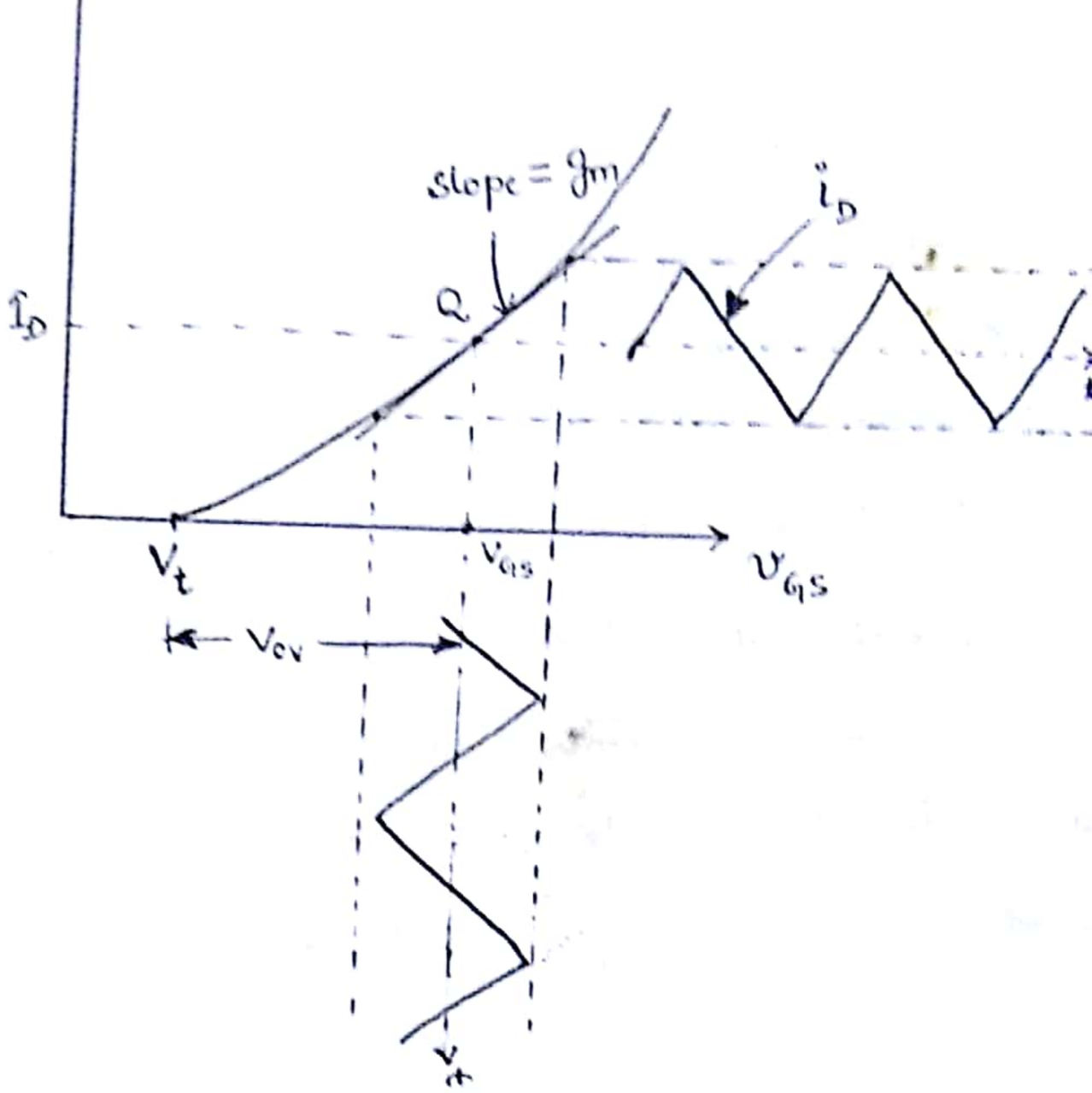
$$i_D \simeq I_D + i_d \qquad \left[i_d = k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} \right]$$

$$i_d = k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

$$g_m \equiv \frac{i_d}{v_{gs}} = k_n' \frac{W}{L} (V_{GS} - V_t)$$

$$g_m = k_n' \frac{W}{L} V_{ov} \longrightarrow \text{MOSFET Transconductance}$$

Which is equal to the slope of $i_D - v_{GS}$ characteristics at Q-point.



Or

$$g_m \equiv \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS} = V_{GS}}$$

Voltage - Gain $\longrightarrow$

$$v_D = V_{DD} - i_D R_D$$

$$v_D = V_{DD} - R_D (I_D + i_d)$$

$$v_D = V_D - R_D i_d$$

$$v_d = -i_d R_D = -g_m v_{gs} R_D$$

(Signal component at drain)

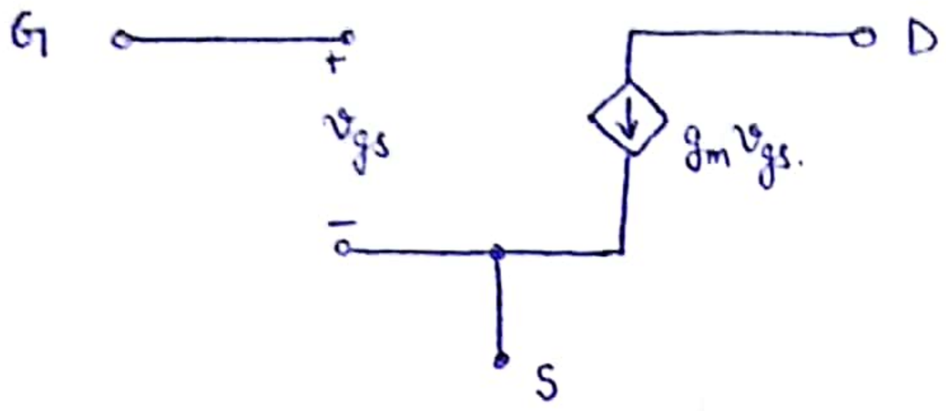
$$A_v = \frac{v_d}{v_{gs}} = -g_m R_D$$

$v_D \geq v_G - V_t \longrightarrow$ Saturation region operation.

$\hookrightarrow v_{D\,min} \geq v_G - V_t$

$v_{gs} << 2(V_{GS} - V_t) \longrightarrow$ To ensure linear amplification.

Small Signal Equivalent circuit Models:- FET behaves like a voltage-controlled current source because it accepts a signal v_{gs} as an i/p b/w gate & source and provides a current $g_m v_{gs}$ at the drain terminal.



A MOSFET can be replaced by the circuit shown above because its i/p resistance is infinite ideally and o/p resistance is infinite also (very high), but only for small signal operation. So we can name this circuit as small signal equivalent circuit or small signal model of MOSFET.

But take a look at the circuit, In this circuit the drain current '$g_m v_{gs}$' is independent of the drain voltage which is a contradiction b/w what we have studied so far. i_d depends linearly on v_{DS}, which is modelled by a finite resistance r_o b/w drain & source.

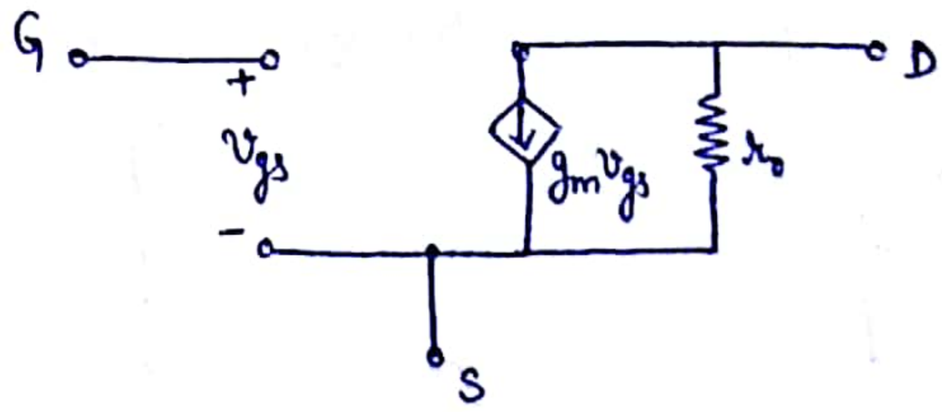
$$r_o = \frac{|V_A|}{I_D}$$

$V_A = 1/\lambda$ → process technology parameter

$V_A \propto$ channel length 'L'

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{ov})^2$$

→ over drive voltage



* Small signal parameters g_m, r_o depend upon DC-bias point.

voltage-gain expression for small signal model/circuit is given by -

$$\frac{v_d}{v_{gs}} = A_v = -g_m (R_D \| r_o)$$

Transconductance :-

$$g_m = \frac{i_d}{v_{gs}} = k_n' \frac{W}{L}(V_{GS} - V_t) = k_n' \frac{W}{L}\{V_{ov}\}$$

$g_m' \propto k_n' \left(\frac{W}{L}\right)$ ⟶ $g_m \uparrow$ $W \uparrow, L \downarrow$ [Device must be short & wide]

$g_m \propto V_{ov}$ ⟶ $V_{ov} \uparrow$ reduces the allowable voltage swing at drain.

$$(V_{GS} - V_t)^2 = \frac{2I_D}{k_n'(W/L)}$$

$$g_m = \sqrt{2k_n'}\sqrt{W/L}\sqrt{I_D}$$

and. $$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{ov}}$$

T- Equivalent circuit model :-

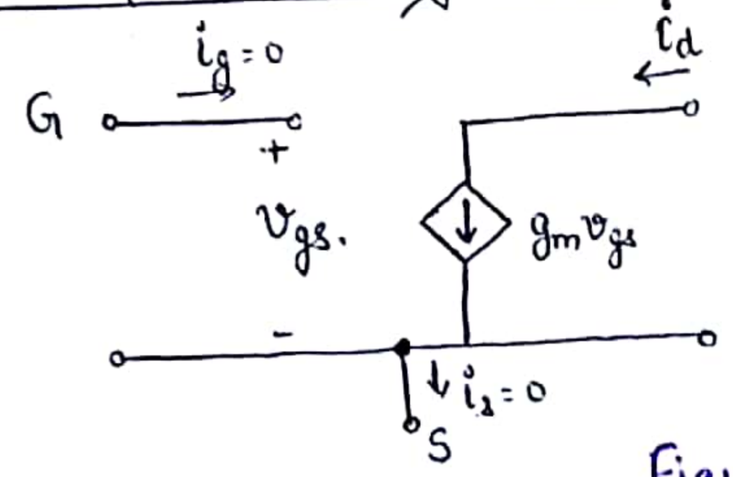


Figure - 1

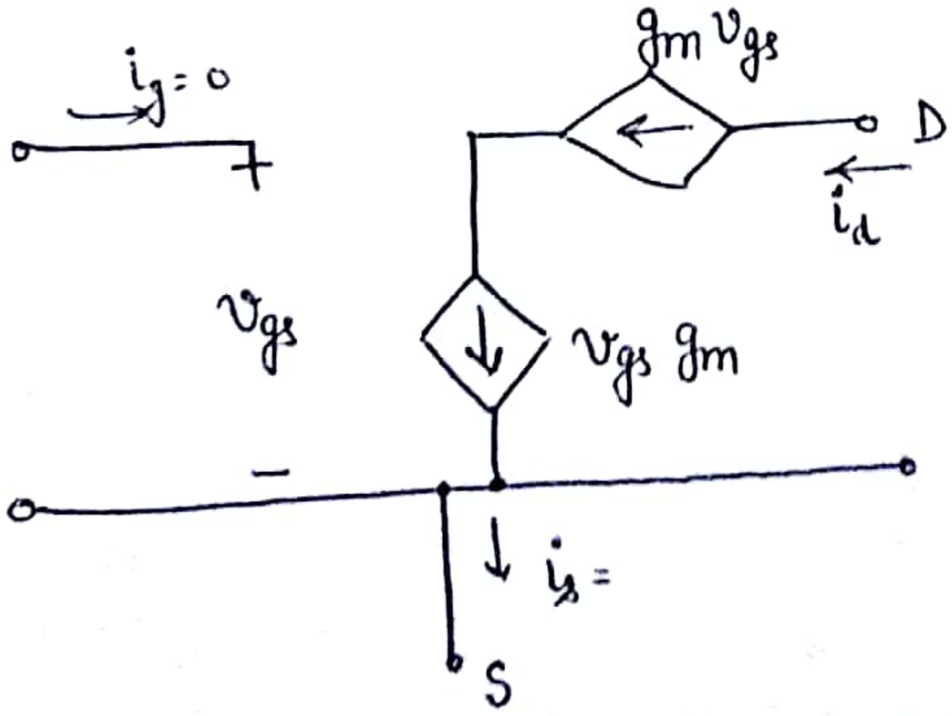
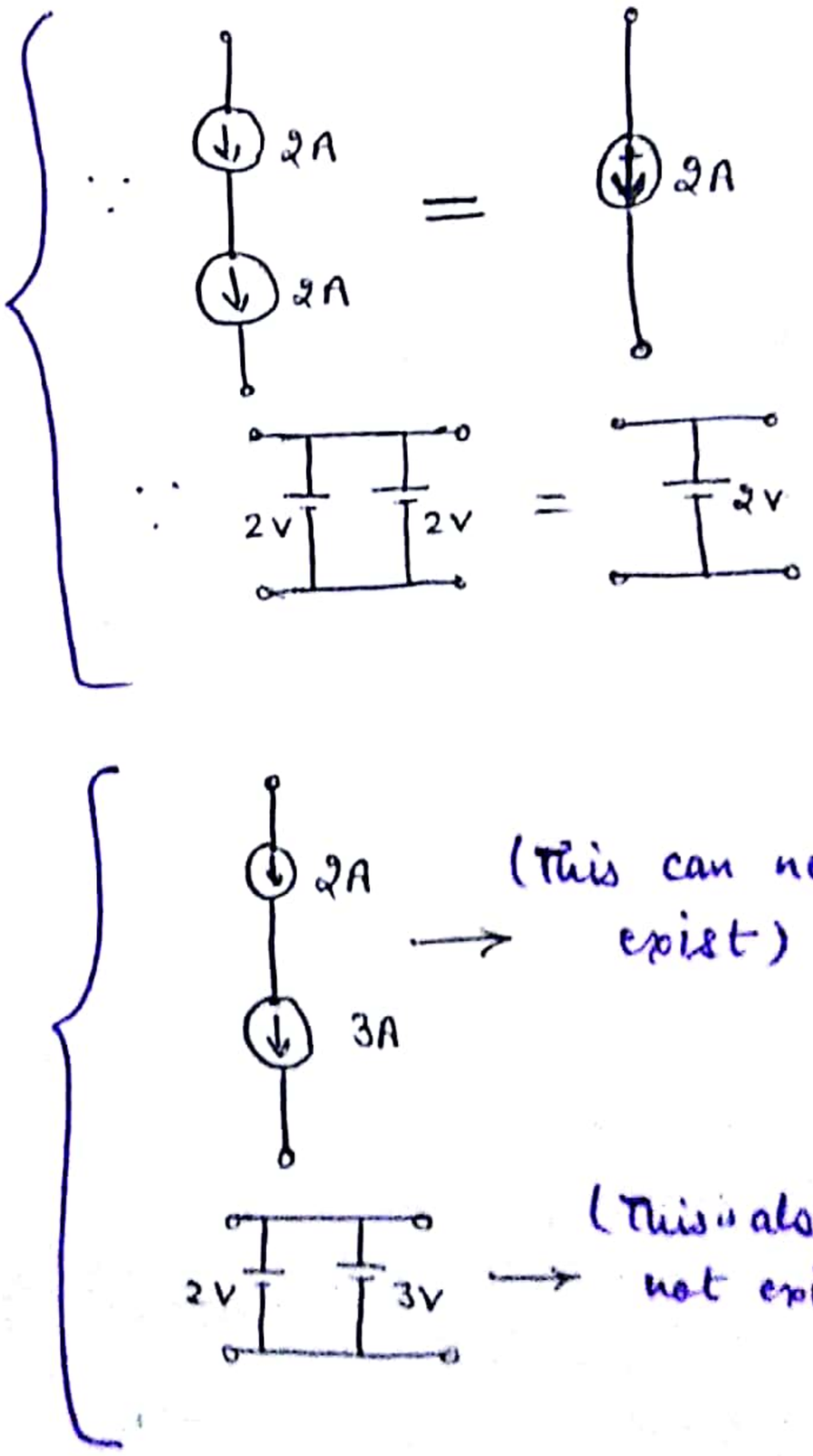


Figure - 2



Since a current source has infinite resistance in b/w its both ends and the MOSFET has an infinite i/p impedance also, we can convert the previous circuits as —

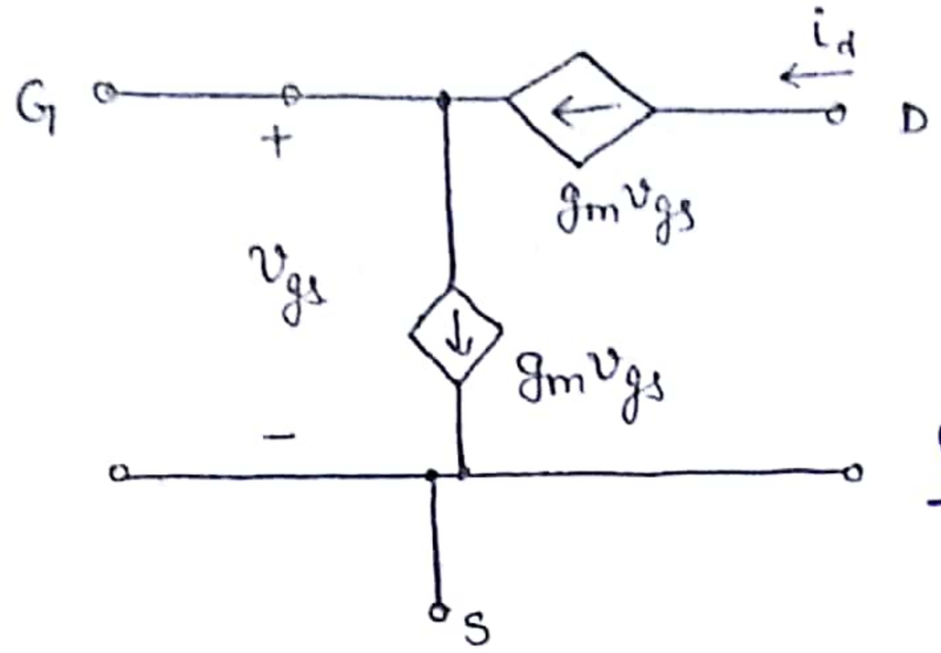


Figure - 3

This circuit can be represented as —

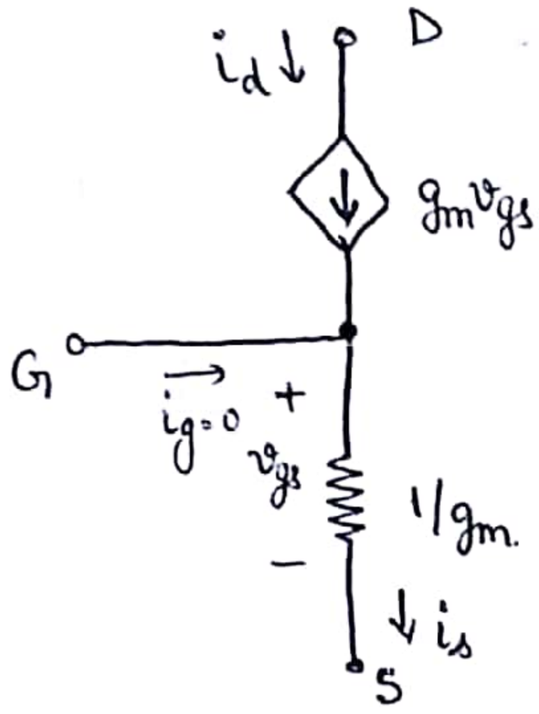


Figure - 4

And if there exist a resistance b/w Drain to Source (r_o) then this above given circuit can be converted / represented as —

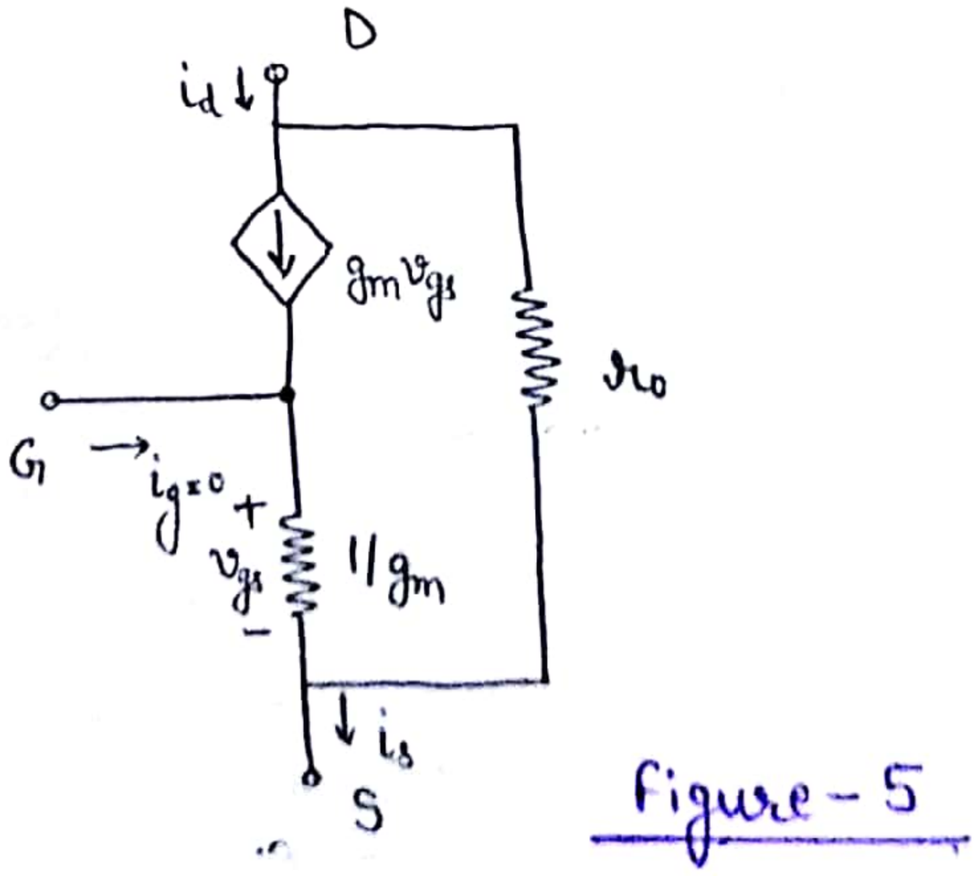


Figure - 5

Single-Stage MOS Amplifiers :—

Before going to the MOS amplifiers let us first check the various types of amplifiers exists and also their configurations.

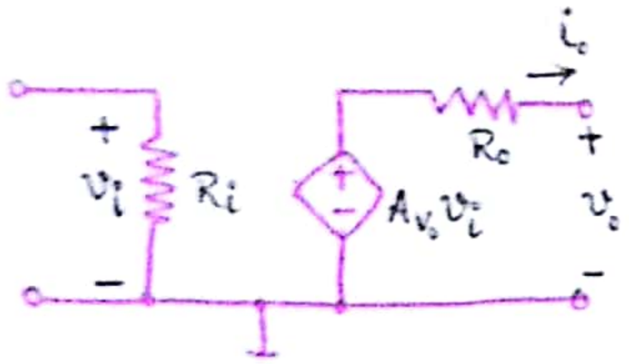


Fig (1)→ Voltage Amplifier

open circuit voltage gain (A_{v_o})

$$A_{v_o} = \frac{v_o}{v_i}\Big|_{i_o=0} \quad (V/V)$$

$$\left\{\begin{array}{l} R_i = \infty \\ R_o = 0 \end{array}\right\}$$ Ideally

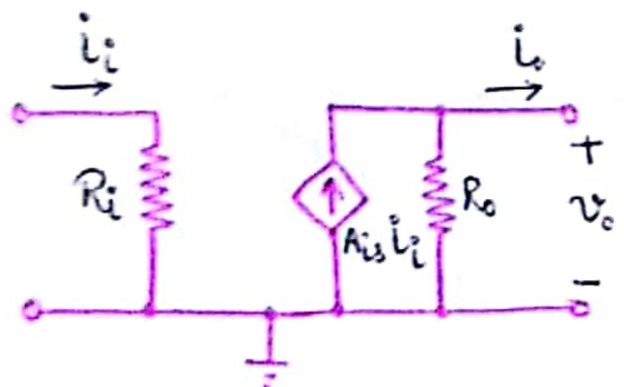


Fig (2)→ Current Amplifier

Short circuit current gain (A_{is})

$$A_{is} = \frac{i_o}{i_i}\Big|_{v_o=0} \quad (A/A)$$

$$\left\{\begin{array}{l} R_i = 0 \\ R_o = \infty \end{array}\right\}$$ Ideally

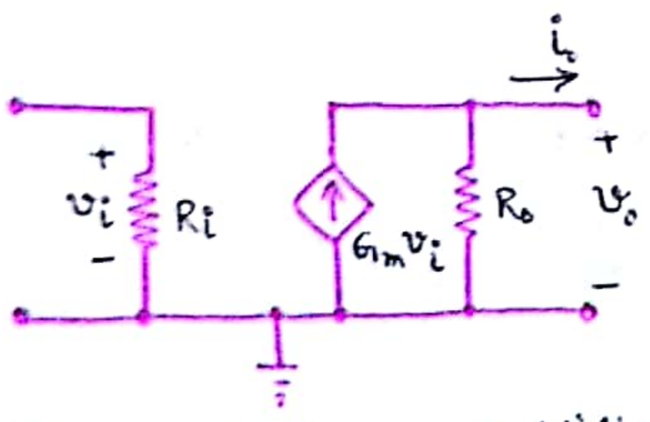


Fig (3)→ Transconductance Amplifier

Short circuit Transconductance (G_m)

$$G_m = \frac{i_o}{v_i}\Big|_{v_o=0} \quad (A/V)$$

$$\left\{\begin{array}{l} R_i = \infty \\ R_o = \infty \end{array}\right\}$$ Ideally

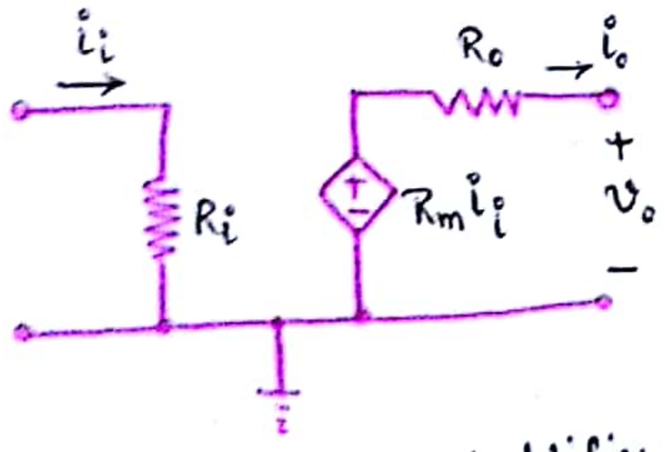


Fig (4)→ Transresistance Amplifier

open circuit Transresistance (R_m)

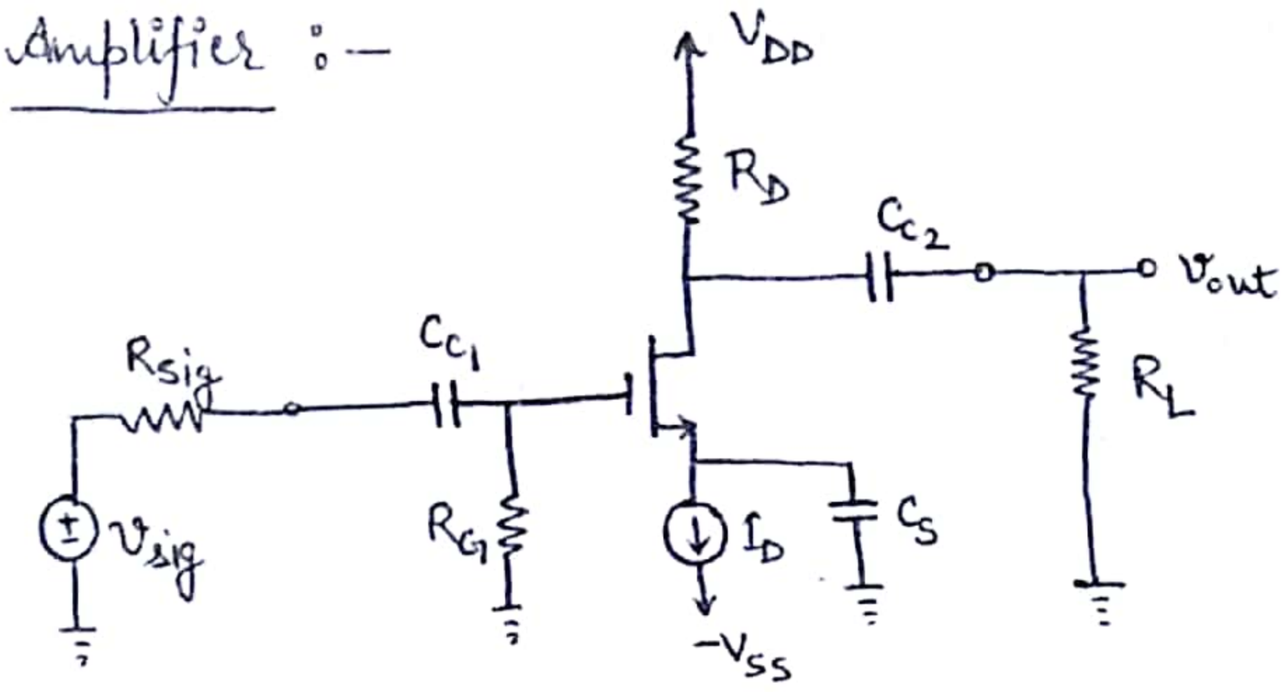
$$R_m = \frac{v_o}{i_i}\Big|_{i_o=0} \quad (V/A)$$

$$\left\{\begin{array}{l} R_i = 0 \\ R_o = 0 \end{array}\right\}$$ Ideally

3 basic configurations —

1- common - source Amplifier
2- common - Gate Amplifier
3- common - Drain Amplifier

Common Source Amplifier :-



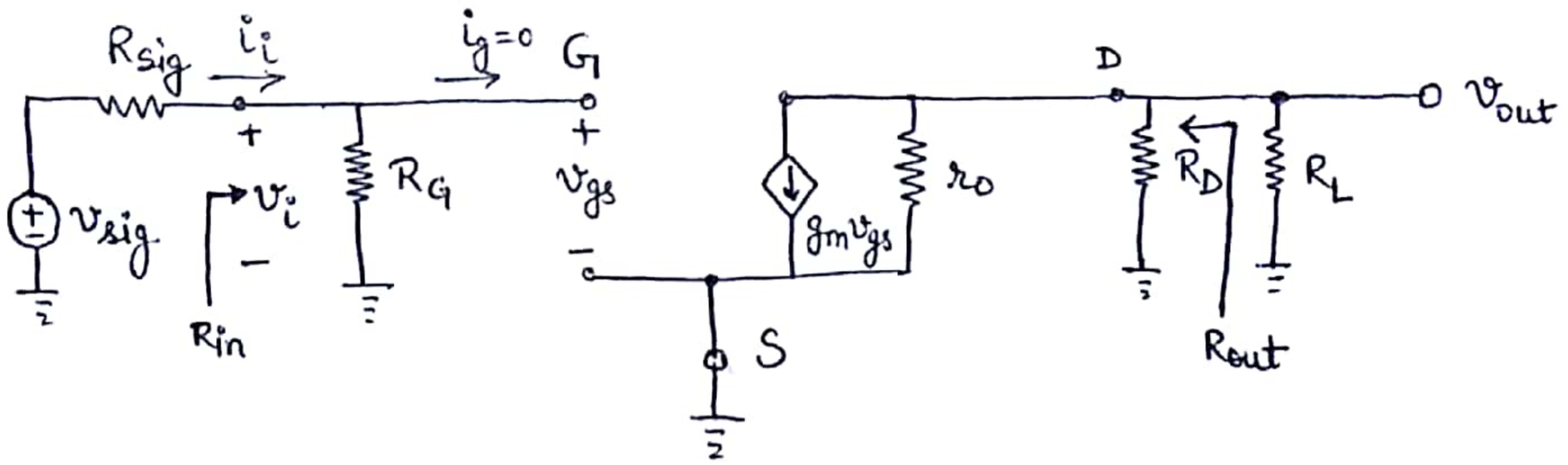


Fig :- Equivalent circuit of C-S amplifier for small signal.

C_{C_1} & C_{C_2} → Coupling capacitors → Block DC components of current.

C_S → Bypass capacitor → Provide low o/p resistance

$$i_g = 0$$

$$v_i = i_i R_G$$

$$v_{sig} = i_i R_{sig} + i_i R_G \quad \Rightarrow \quad i_i = \frac{v_{sig}}{R_{sig} + R_G}$$

$$v_i = \frac{R_G}{R_{sig} + R_G} v_{sig}.$$

$$\boxed{R_{in} = R_G}$$

$$R_G >> R_{sig} \longrightarrow v_i \cong v_{sig}$$

$$v_{gs} = v_i \cong v_{sig}$$

$$v_{out} = -g_m v_{gs} (r_o \,||\, R_D \,||\, R_L)$$

voltage gain $\boxed{A_v = \frac{v_{out}}{v_{gs}} = -g_m (r_o \| R_D \| R_L)}$ → MOSFET's gain

If $R_L \equiv \infty$ → open circuit

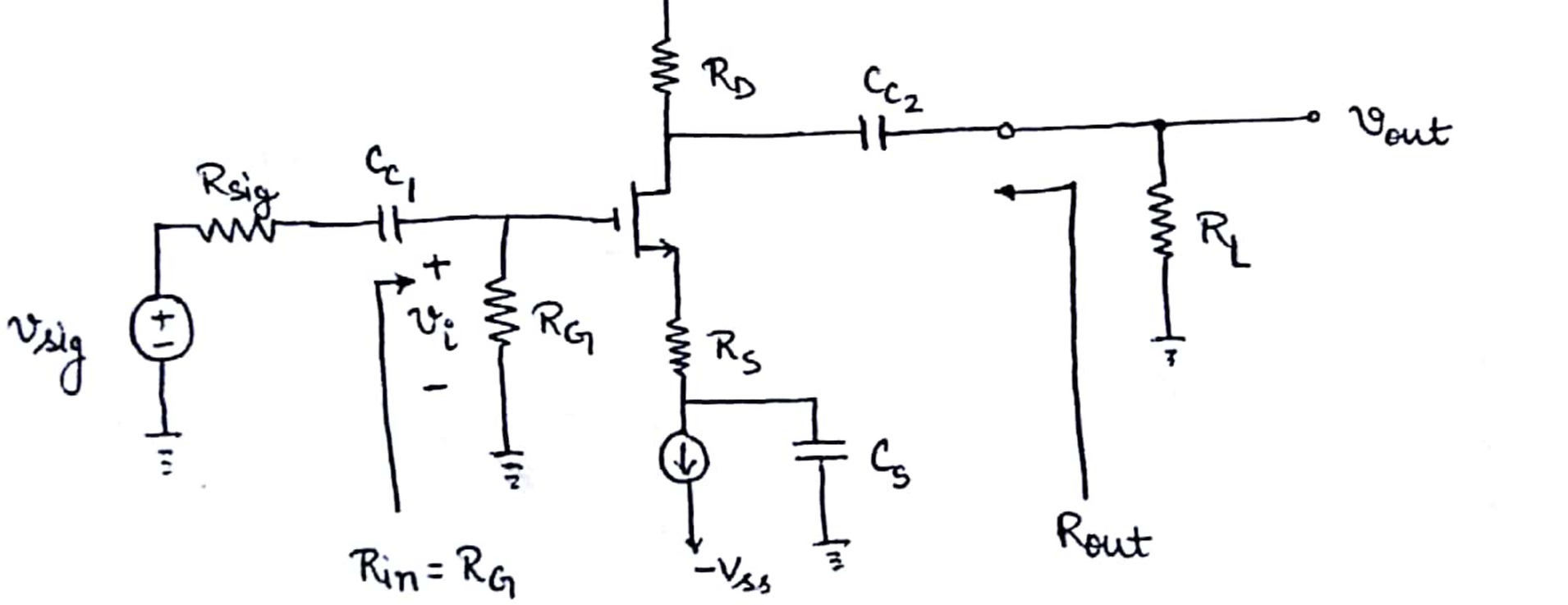
open circuit voltage gain $\boxed{A_{v_o} = -g_m (r_o \| R_D)}$

overall voltage gain G_v is given by $\frac{v_{out}}{v_{sig}}$

$$\boxed{G_v = \frac{v_{out}}{v_{sig}} = -\frac{R_G}{R_G + R_{sig}} g_m (r_o \| R_D \| R_L)}$$

$$\boxed{R_{out} = r_o \| R_D}$$

Common-Source Amplifier with a source Resistance :—



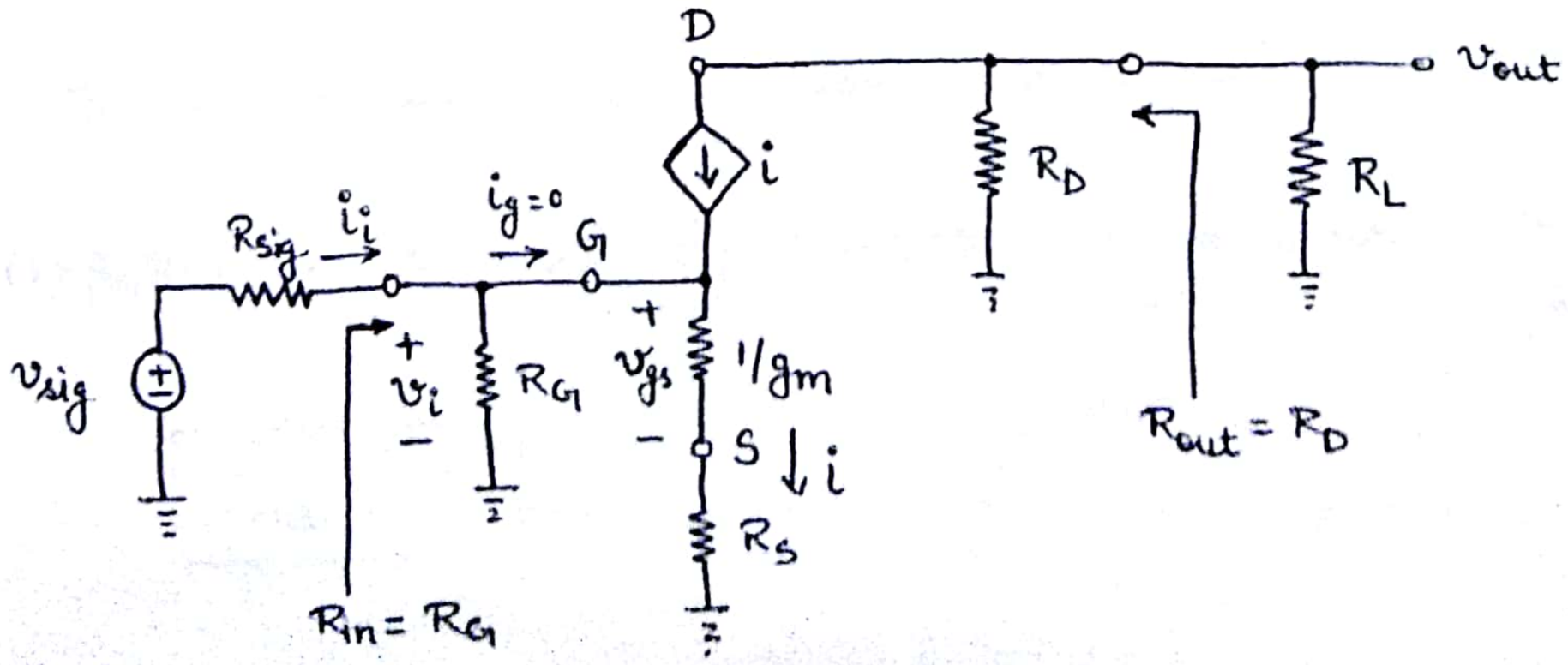


Fig :- Equivalent ckt for C-S Amplifier with source Resistance

$$\boxed{R_{in} = R_f = R_G}$$

$$v_i = \frac{R_G}{R_{sig} + R_G} v_{sig}$$

$$v_{gs} = \frac{1/g_m}{\frac{1}{g_m} + R_S} v_i = \frac{v_i}{1 + g_m R_S}$$

$$i_d = i = \frac{v_i}{\frac{1}{g_m} + R_S} = \frac{g_m v_i}{1 + g_m R_S}$$

$$v_{out} = - i_d (R_D \parallel R_L) = \frac{- g_m (R_D \parallel R_L)}{(1 + g_m R_S)} v_i$$

voltage gain $\boxed{A_v = \frac{- g_m (R_D \parallel R_L)}{1 + g_m R_S}}$

$$\boxed{A_{v_o} = - \frac{g_m R_D}{1 + g_m R_S}}$$

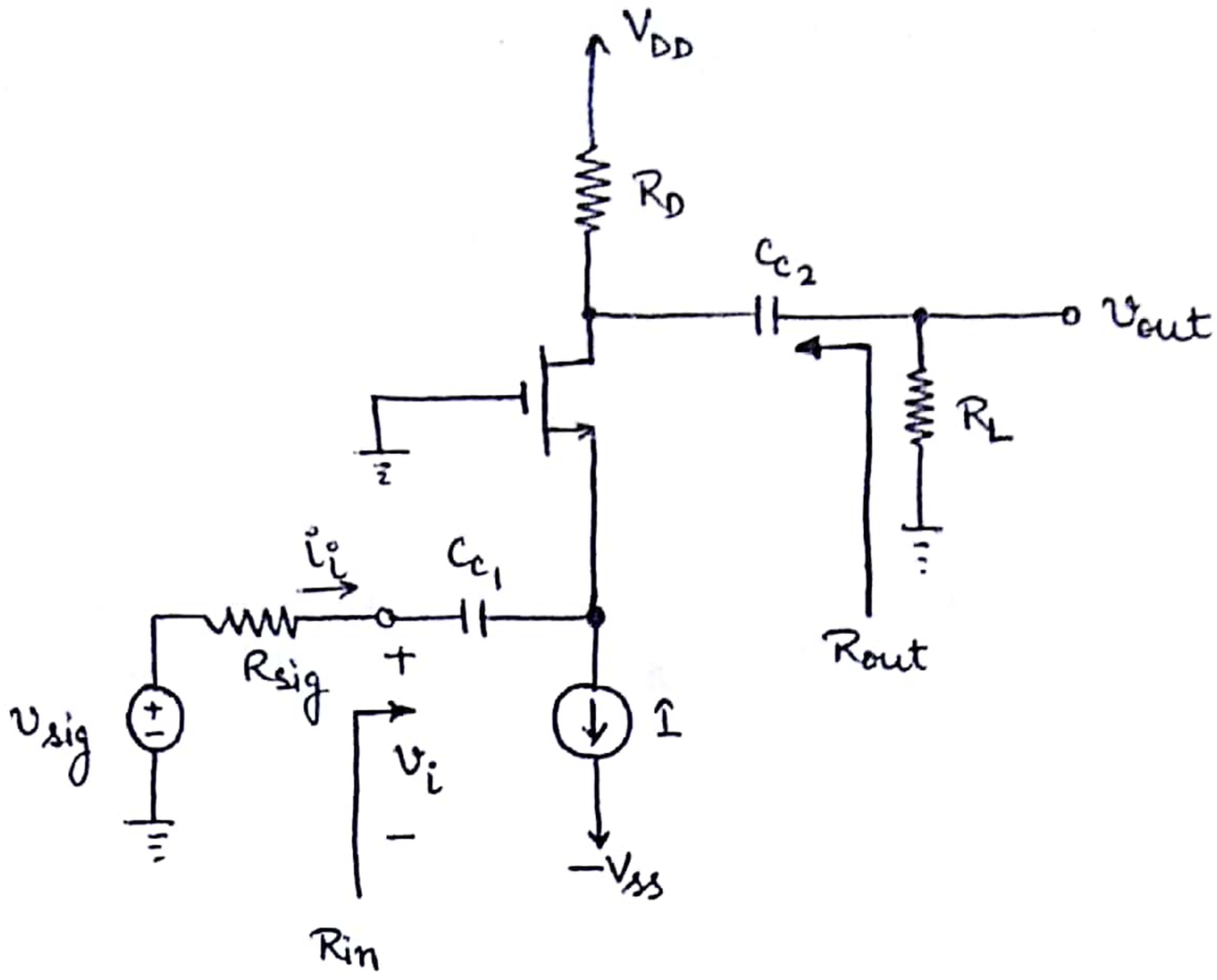
overall voltage gain $\boxed{(G) = \frac{- R_G}{R_G + R_{sig}} \cdot \frac{g_m (R_D \parallel R_L)}{1 + g_m R_S}}$

$R_S \rightarrow$ Source degeneration resistance

$(1 + g_m R_S) \rightarrow$ Amount of feedback (discuss later in feedback techniques)

$$\boxed{R_{out} = R_D}$$

Common - Gate Amplifier :—



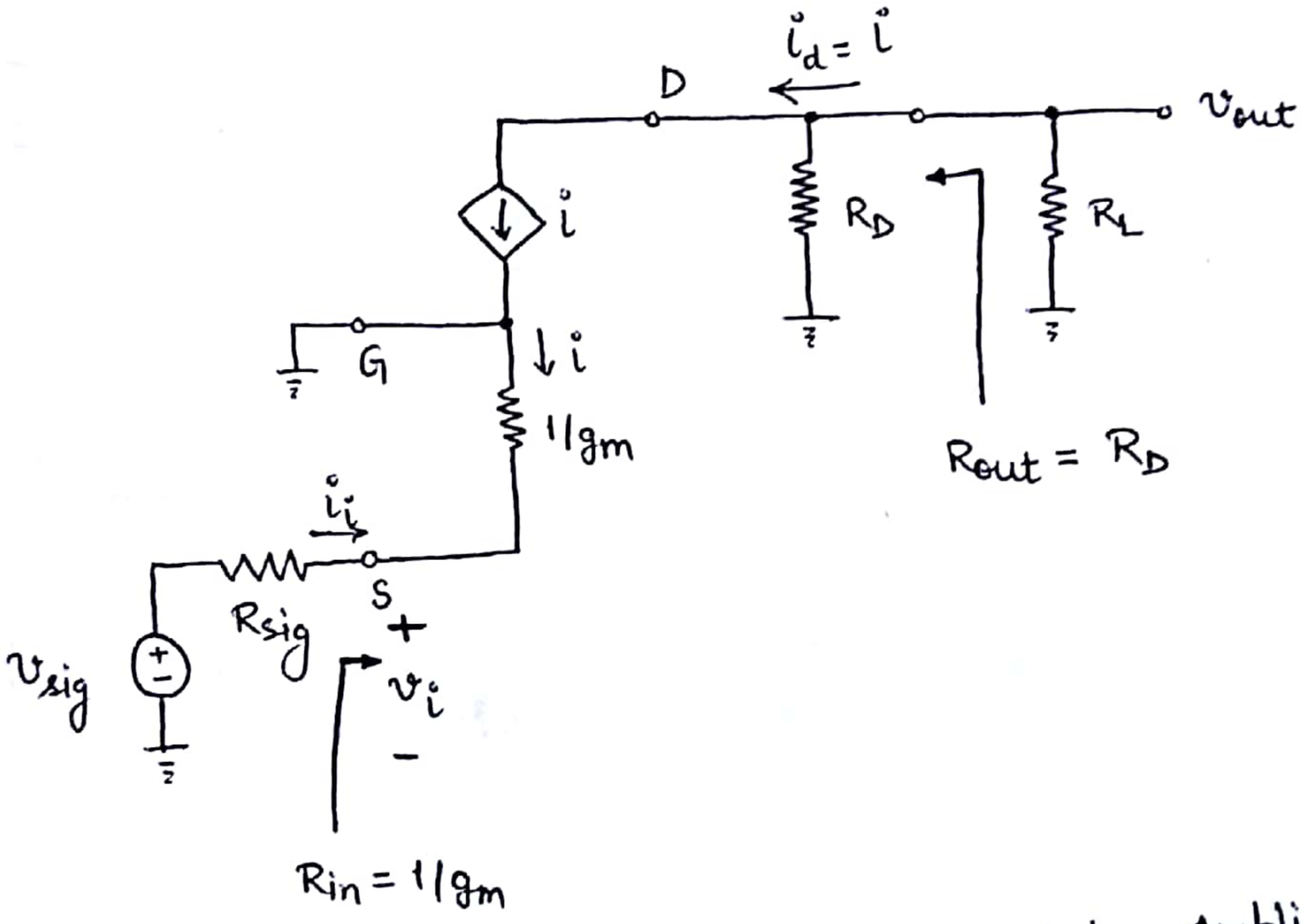


Fig :— Equivalent circuit for Common Gate Amplifier.

$R_{in} = 1/g_m.$

$$v_i = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig} = \frac{1/g_m}{\frac{1}{g_m} + R_{sig}} v_{sig} = \frac{1}{1 + g_m R_{sig}} v_{sig}.$$

To keep $v_i \cong v_{sig}$ [To prevent signal loss] $\frac{1}{g_m} >> R_{sig}.$

$$i_i = \frac{v_i}{R_{in}} = \frac{v_i}{1/g_m} = g_m v_i$$

$$i_d = i = -i_i = -g_m v_i$$

$$v_{out} = -i_d (R_D \| R_L) = g_m (R_D \| R_L) v_i$$

$$\boxed{A_v = g_m (R_D \| R_L)}$$

$$\boxed{A_{v_0} = g_m R_D}$$

$$G_I = \frac{R_{in}}{R_{in} + R_{sig}} A_v = \frac{1/g_m}{1/g_m + R_{sig}} A_v$$

$$= \frac{A_v}{1 + g_m R_{sig}}$$

$$\boxed{G_I = \frac{g_m (R_D \| R_L)}{1 + g_m R_{sig}}}$$

$$\boxed{R_{out} = R_D}$$

$$i_i = i_{sig} \frac{R_{sig}}{R_{sig} + R_{in}} = \frac{R_{sig}}{R_{sig} + 1/g_m} i_{sig}$$

$R_{sig} >> 1/g_m$

$i_i \equiv i_{sig}$ ⟶ This make the above circuit a 'current follower' or 'unity gain current amplifier'.

Common-Drain or Source-Follower Amplifier :-

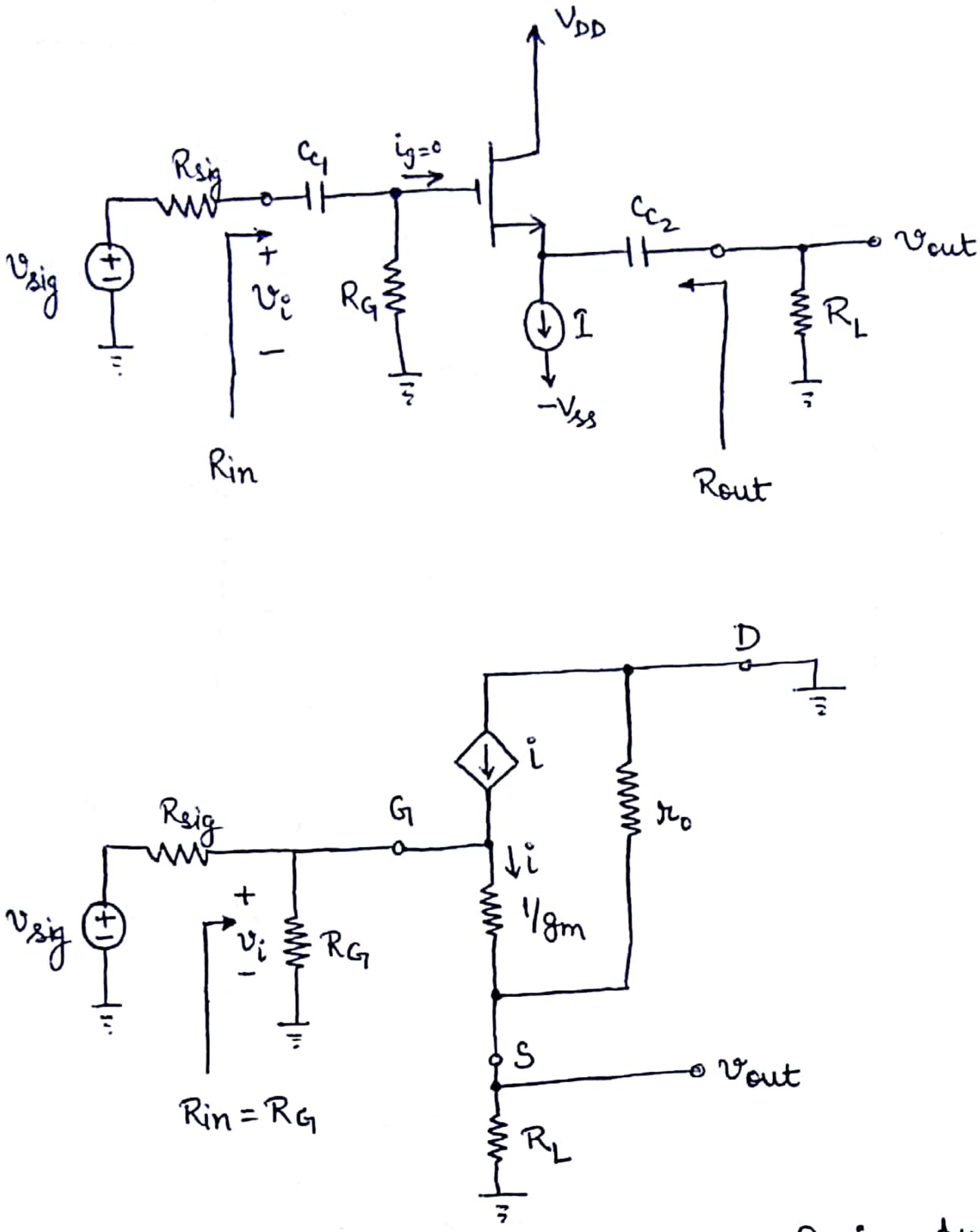


fig- Equivalent circuit for common-Drain Amplifier

$$\boxed{R_{in} = R_G}$$

$$v_i = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig} = \frac{R_G}{R_G + R_{sig}} v_{sig}$$

$R_G >> R_{sig} \longrightarrow v_i \cong v_{sig}$.

$$v_{out} = v_i \frac{(R_L \| r_o)}{\frac{1}{g_m} + (R_L \| r_o)}$$

$$\boxed{A_v = \frac{R_L \| r_o}{(R_L \| r_o) + 1/g_m}}$$

$$A_{v_0} = \frac{r_o}{r_o + 1/g_m.}$$

$r_o >> 1/g_m \longrightarrow A_{v_0} \simeq 1$

$r_o >> R_L$ (normally)

$$A_v \simeq \frac{R_L}{R_L + 1/g_m.}$$

overall gain G

$$G = \frac{R_G}{R_G + R_{sig}} \cdot \frac{(R_L \| r_o)}{(R_L \| r_o) + \frac{1}{g_m.}}$$

$R_G >> R_{sig.}$

$r_o >> 1/g_m.$

$r_o >> R_L$

$$G \simeq 1$$

$$R_{out} = \frac{1}{g_m} \| r_o$$

$r_o >> 1/g_m \longrightarrow R_{out} \simeq 1/g_m.$

MOSFET's Internal Capacitances :- Two types of internal capacitance in the MOSFET.

(i) Gate Capacitive Effect → Gate electrode forms a parallel plate capacitor with the channel and oxide layer plays a role of dielectric here. This capacitance is denoted by C_{ox}. This capacitance has been discussed in the derivation of the $i_D - v_{DS}$ relationship.

(ii) Source-body & drain-body depletion layer capacitances → Capacitances of reverse-bias p-n junctions formed by n^+-type source and p-substrate and n^+-type drain and p-substrate.

So there will be 5 capacitances in total —
C_{gs}, C_{gd}, C_{gb}, C_{sb}, C_{db} (Subscripts indicates the location)

$$C_{gs} = C_{gd} = \frac{1}{2} WL C_{ox} \longrightarrow \text{Triode Region}$$

$$\left.\begin{aligned} C_{gb} &= WL C_{ox} \\ C_{gs} &= C_{gd} = 0 \end{aligned}\right\} \longrightarrow \text{Cut-off Region.}$$

$$\left.\begin{aligned} C_{gs} &= \frac{2}{3} WL C_{ox} \\ C_{gd} &= 0 \end{aligned}\right\} \longrightarrow \text{Saturation Region}$$

$$C_{sb} = \frac{C_{sb_0}}{\sqrt{1 + \frac{V_{SB}}{V_0}}}$$

$$C_{db} = \frac{C_{db_0}}{\sqrt{1 + \frac{V_{DB}}{V_0}}}$$

C_{sb_0} → C_{sb} at zero body-source bias.

V_{SB} → Reverse bias voltage's magnitude b/w S-B.

V_0 → Built-in voltage

C_{db_0} → C_{db} at zero drain-body bias.

V_{DB} → Reverse bias voltage's magnitude b/w D-B.

High frequency MOSFET model :-

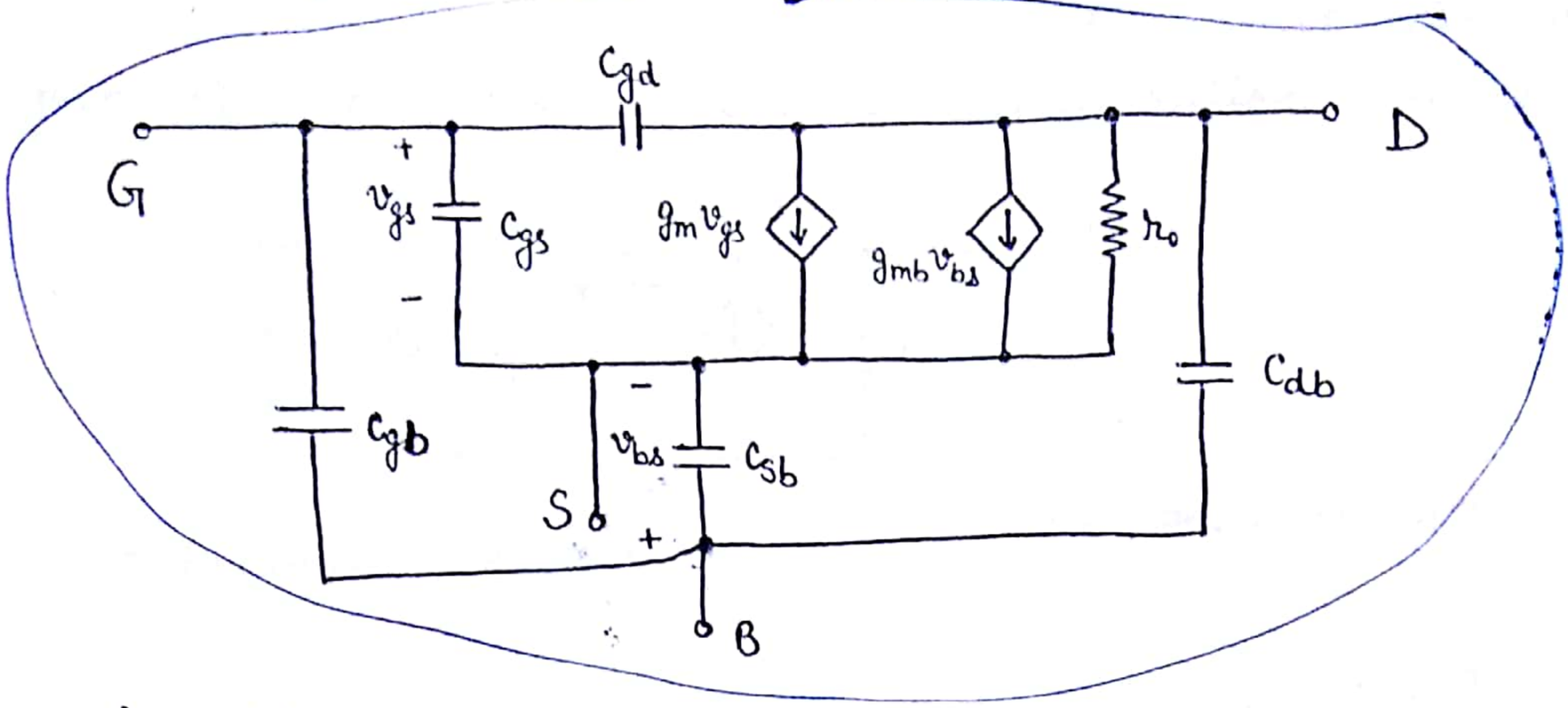
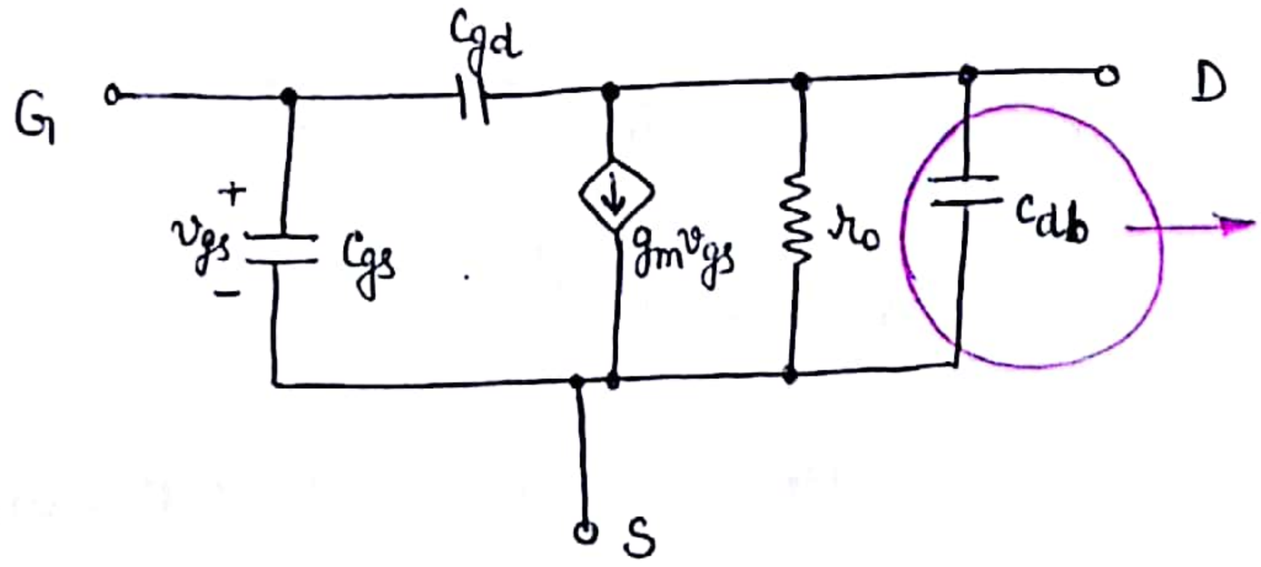


Fig- High-freq. equivalent circuit model for MOSFET.

This circuit model can be used to predict the high-frequency response of MOSFET amplifiers, however it is quite complex for manual analysis.

The above model gets simplified considerably when the source & body connected together. In this case model can be represented as —



→ This can also be neglected for the simplicity of the manual analysis.

C_{gd} → is also small but plays a vital role in determining the high frequency response of the amplifiers.

MOSFET → unity-gain frequency (f_T) → It is the freq. at which the short circuit current gain of the common-source configuration becomes unity.

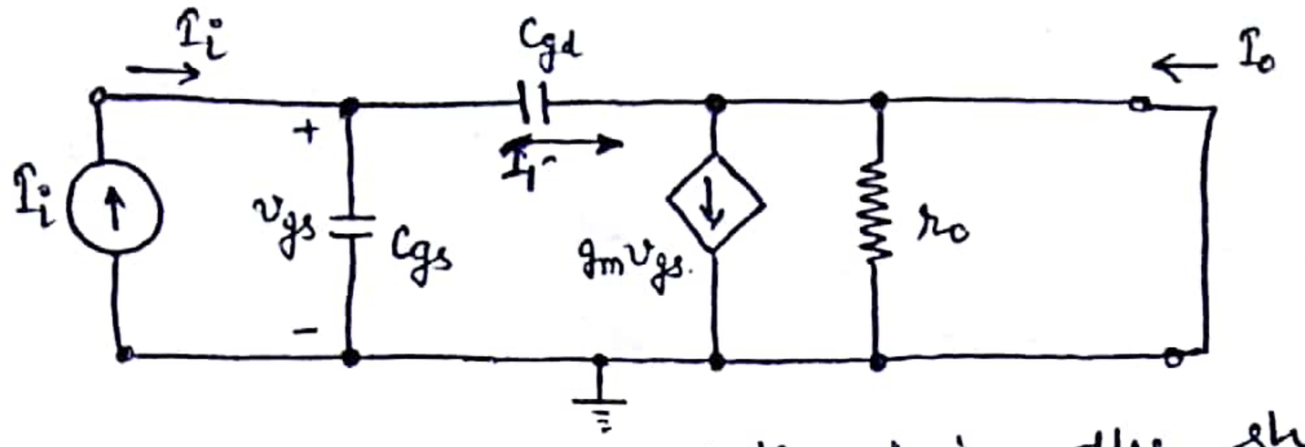


Fig → Equivalent ckt for determining the short ckt gain I_o/I_i of MOSFET.

$$I_o = g_m v_{gs} - s C_{gd} v_{gs}. \qquad \left[\because I_1 = s C_{gd}.(v_{gs} - 0)\right.$$

If C_{gd} is small for all frequencies of intrest then we can neglect this term. Now

$$I_o \cong g_m v_{gs}. \qquad \text{——} (1)$$

Now at the o/p terminal

$$I_i = s C_{gs} v_{gs} + s C_{gd} v_{gs}$$

$$I_i = s v_{gs} (C_{gd} + C_{gs})$$

$$v_{gs} = I_i / s(C_{gs} + C_{gd})$$

Putting this in eq^n (1) we get —

$$I_o \cong g_m I_i / s(C_{gs} + C_{gd})$$

$$\boxed{\frac{I_o}{I_i} = \frac{g_m}{s(C_{gs} + C_{gd})}} \rightarrow \text{Expression for short circuit current gain.}$$

$$|A_{is}| = \left|\frac{I_o}{I_i}\right| = \frac{g_m}{\omega (C_{gs} + C_{gd})}$$

@ $\omega = \omega_T$; $A_{is} = 1$ → $\boxed{\omega_T = \frac{g_m}{C_{gs} + C_{gd}}} \Rightarrow \boxed{f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}}$

Frequency Response of CS-Amplifier :- Gain of the MOSFET amplifier depends upon the frequency of the input signal.

3-frequency Bands :-

$$G = A_M = \frac{V_o}{V_{sig}} = -\frac{R_G}{R_G + R_{sig}} g_m (r_o \| R_D \| R_L)$$

This gain falls off at signal frequencies below and above midband, and is almost constant over a wide frequency band (midband). This is shown graphically in the figure given below.

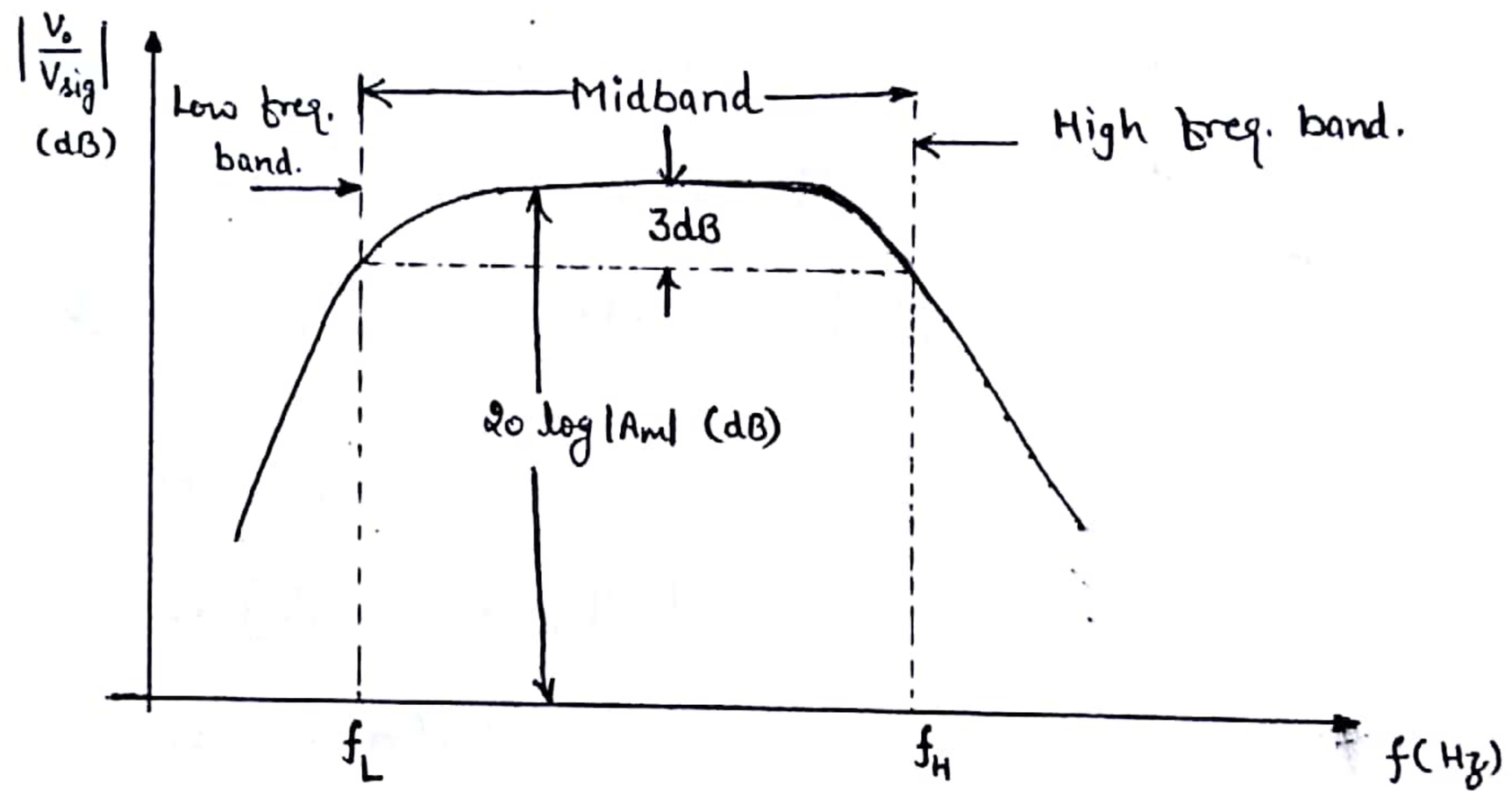


fig:- Freq. Response of the amplifier

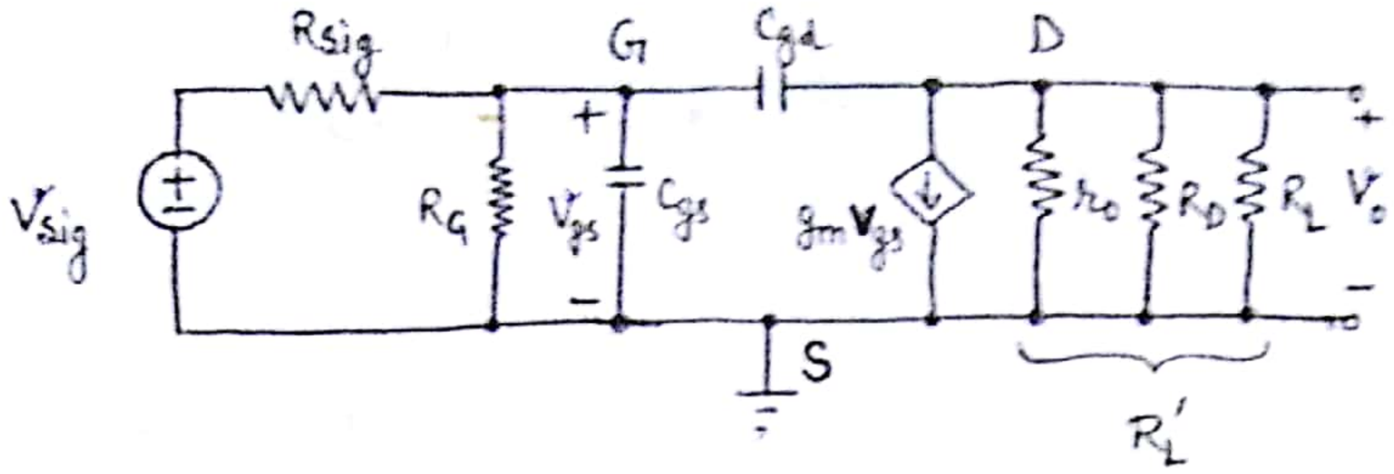
* For the freq. lower than the f_L or in low freq. band gain falls-off because of the fact that even though C_{C_1}, C_{C_2}, C_S are large capacitors (μf-range), as the signal freq. is reduced, their impedence increase, so they no longer behave as short circuits.

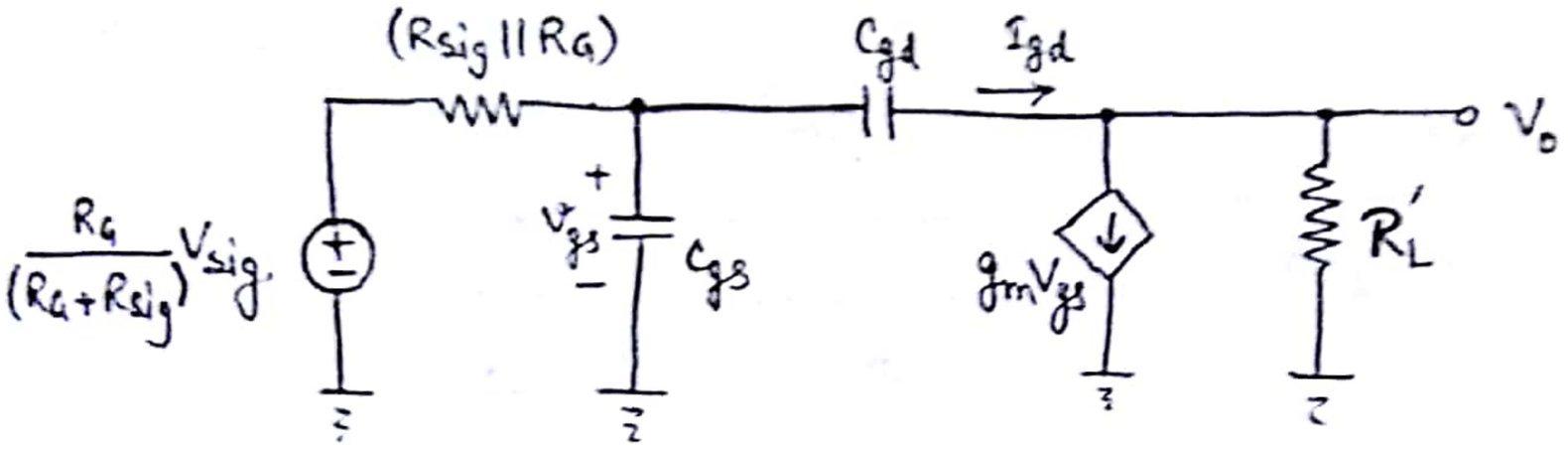
* For the high freq. band ($>F_H$) the gain falls off due to fact that C_{gs}, C_{gd} are although very small (in pf-range), but their impedence decrease at the higher frequencies, thus they can no longer considered as open circuits.

3-dB Bandwidth = $BW \equiv f_H - f_L$ → if $f_L \ll f_H$ → $BW \simeq f_H$ (usually)

Gain BW product $GB = |A_M| BW$

High-Frequency Response :-





Current in the load resistor R_L' is given by $(g_m V_{gs} - I_{gd})$ so the voltage across it or V_o is approximated by –

$$V_o = -R_L' (g_m V_{gs} - I_{gd}) \cong -g_m V_{gs} R_L' \quad \text{——— (A)}$$

$$I_{gd} = s C_{gd} (V_{gs} - V_o)$$

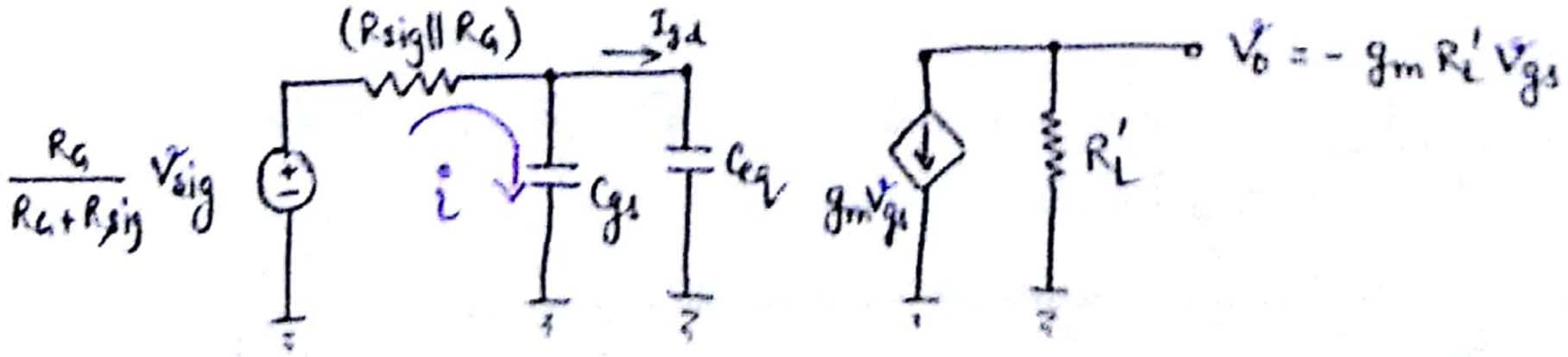
$$= s C_{gd} \left[V_{gs} - (-g_m V_{gs} R_L')\right]$$

$$= s C_{gd} (1 + g_m R_L') V_{gs}$$

Now, the existence of C_{gd} is only through I_{gd}. Therefore we can replace C_{gd} by an equivalent capacitance C_{eq} b/w gate & ground as long as C_{eq} draws a current equal to I_{gd}.

$$s C_{eq} V_{gs} = s C_{gd} (1 + g_m R_L') V_{gs}$$

$$\therefore \boxed{C_{eq} = C_{gd} (1 + g_m R_L')}$$



By applying KVL in the i/p loop

$$\frac{R_G}{R_G + R_{sig}} v_{sig} = i\,(R_{sig} \| R_G) + \frac{i}{s(C_{gs} + C_{eq})}$$

$$v_{gs} = i/s(C_{gs} + C_{eq}) \qquad \left\{ R_{sig}' = R_{sig} \| R_G \right\}$$

$$i = \frac{\frac{R_G}{(R_G + R_{sig})} v_{sig}}{\left[R_{sig}' + \frac{1}{s(C_{gs} + C_{eq})} \right]} \Rightarrow \frac{R_G}{(R_G + R_{sig})} V_{sig} \; \frac{s(C_{gs} + C_{eq})}{1 + s(C_{gs} + C_{eq}) R_{sig}'}$$

$$\therefore v_{gs} = \frac{R_G}{(R_G + R_{sig})} V_{sig} \times \frac{s(C_{gs} + C_{eq})}{[1 + s R_{sig}' (C_{gs} + C_{eq})]} \times \frac{1}{s(C_{gs} + C_{eq})}$$

$$v_{gs} = \frac{R_G}{(R_G + R_{sig})} V_{sig} \cdot \frac{1}{[1 + s R_{sig}' (C_{gs} + C_{eq})]} \quad \text{——— (1)}$$

$$v_{gs} = \frac{R_G}{(R_G + R_{sig})} V_{sig} \cdot \frac{1}{(1 + \frac{s}{\omega_0})} \quad \text{——— (2)}$$

comparing eq^n (1) & (2)

$$\omega_0 = 1/(C_{gs} + C_{gd}) R_{sig}'$$

From eq^n (A) we get

$$v_o = -g_m R_L' v_{gs} = -g_m R_L' \frac{R_G}{(R_G + R_{sig})} \cdot \frac{1}{(1 + \frac{s}{\omega_0})} v_{sig}$$

$$\boxed{\frac{v_o}{v_{sig}} = -\frac{R_G}{(R_G + R_{sig})} \cdot (g_m R_L') \frac{1}{(1 + \frac{s}{\omega_0})} = \frac{A_M}{1 + \frac{s}{\omega_H}}} \quad \text{——— (B)}$$

where $\omega_H = \omega_0 = \dfrac{1}{(C_{gs}+C_{eq})\,R'_{sig}}$ → upper 3-dB frequency.

Eq" (B) shows that the high-frequency response will be that of a low-pass STC (Single Time Constt.) network, whose response is shown as shown in figure below—

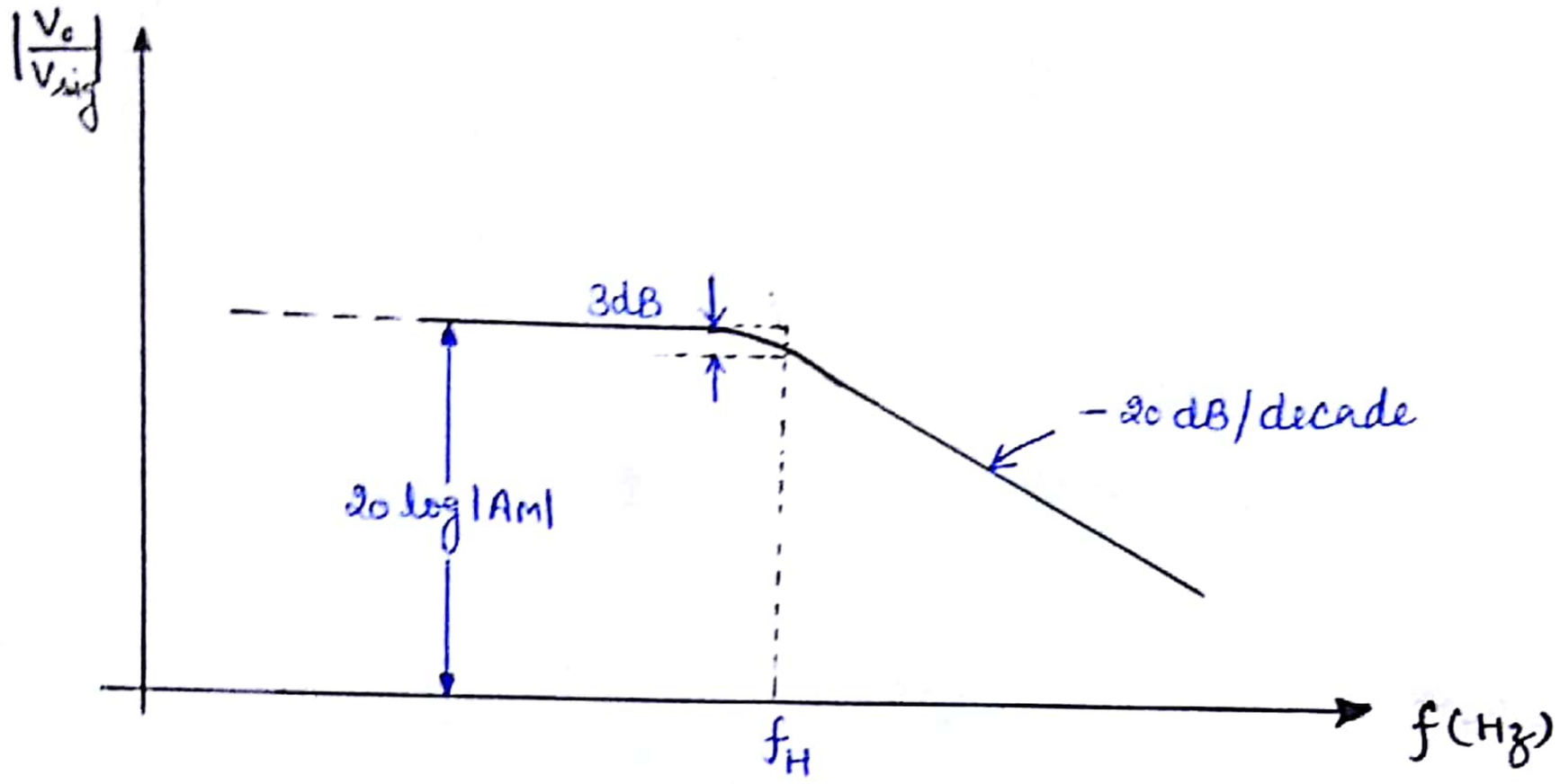


Fig- Freq. Response of Single Time Constt (STC) circuit.

* $R'_{sig} = R_{sig} \,||\, R_a$; R_a is very large usually, $R'_{sig} \cong R_{sig}$

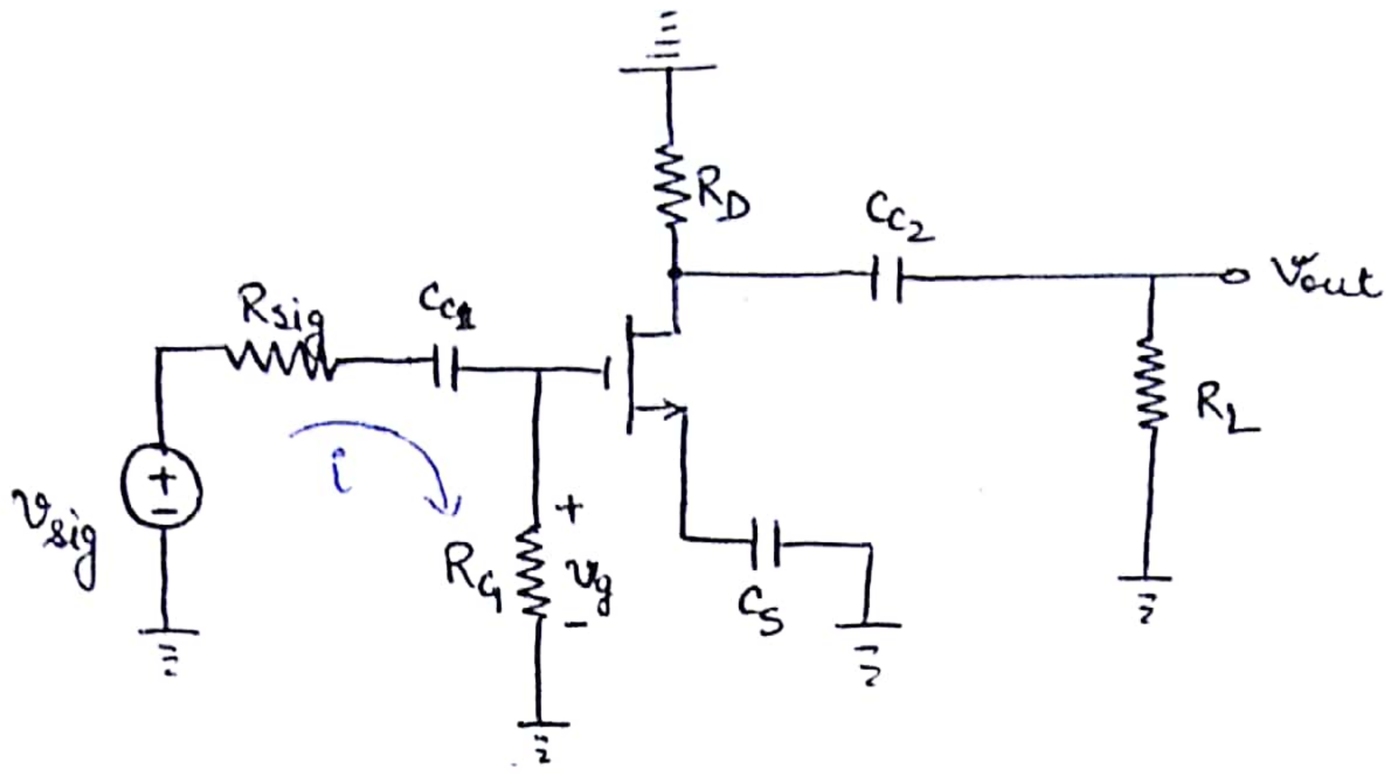
$f_H \propto \dfrac{1}{R'_{sig}}$ → R_{sig} large → (f_H low)

* $C_{eq} = C_{gd} + C_{gd}\, g_m R'_L = C_{gd}(1+g_m R'_L)$ → usually C_{gd} is small but its multiplication with $(1+g_m R'_L)$ turns it into a significant value.

* C_{gd} connected b/w 2 nodes whose voltages are connected by a large negative gain $(-g_m R'_L)$. 'Miller Effect', causes CS-amp' to have large $C_{in} = C_{gs} + C_{gd}(1+g_m R'_L)$ and hence low f_H.

* $(1+g_m R'_L)$ known as 'miller multiplier'.

Low frequency Response :—



$$v_{sig} = i R_{sig} + i R_G + \frac{i}{s C_{C_1}} \Rightarrow i = \frac{v_{sig}}{\left(R_G + R_{sig} + \frac{1}{s C_{C_1}}\right)}$$

$$v_g = i R_G = \frac{R_G}{\left(R_G + R_{sig} + \frac{1}{s C_{C_1}}\right)} v_{sig}$$

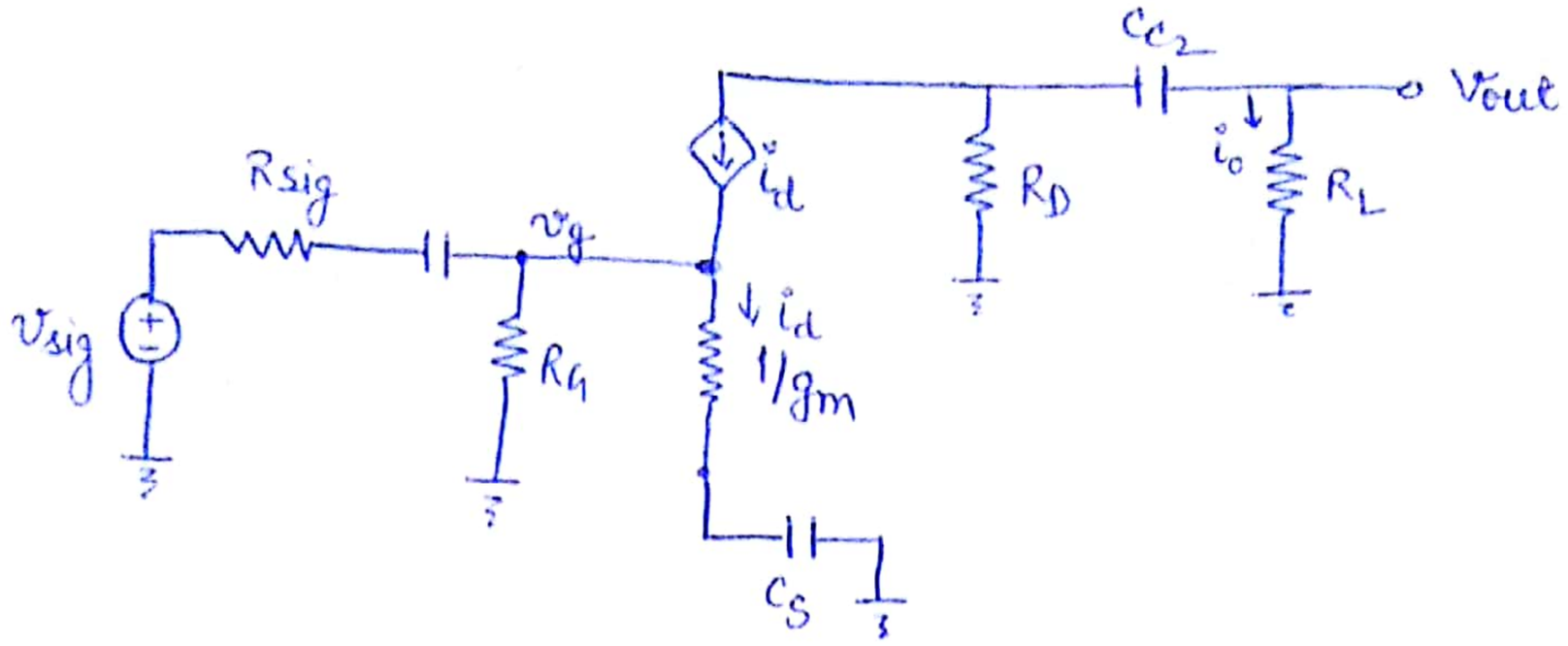
This can also be written as —

$$v_g = v_{sig} \frac{R_G}{(R_G + R_{sig})} \cdot \frac{S}{S + \frac{1}{C_{C_1}(R_G + R_{sig})}}$$

This is the response of STC network of high pass type with break or corner freq. (ω_0)

$$\omega_0 = \frac{1}{C_{C_1}(R_G + R_{sig})} = \omega_{P1}$$

Now converting the above network / circuit into a T-equivalent circuit model, for the analysis of the network, shown on the next page.



$$i_d = \frac{v_g}{\frac{1}{g_m} + \frac{1}{s C_s}} = g_m v_g \frac{s}{s + \frac{g_m}{C_s}}$$

* C_S introduces another freq. dependent factor which is also of high pass type. So another break freq. ω_{P_2} which is given by

$$\omega_{P_2} = \frac{g_m}{C_s}$$

$$i_o = -i_d \cdot \frac{R_D}{(R_D + R_L + \frac{1}{s C_{C_2}})} \longrightarrow \text{current divider rule at the o/p circuit.}$$

$$v_{out} = i_o R_L = -i_d \frac{R_D R_L}{(R_D + R_L)} \cdot \frac{s}{s + \frac{1}{C_{C_2}(R_D + R_L)}}$$

* Thus C_{C_2} introduces a third high pass factor which is discriminated by ω_{P_3}.

$$\omega_{P_3} = \frac{1}{C_{C_2}(R_D + R_L)}$$

overall gain is

$$\boxed{\frac{v_{out}}{v_{sig}} = -\left(\frac{R_G}{R_G + R_{sig}}\right)[g_m(R_D \| R_L)]\left(\frac{s}{s+\omega_{P_1}}\right)\left(\frac{s}{s+\omega_{P_2}}\right)\left(\frac{s}{s+\omega_{P_3}}\right)}$$

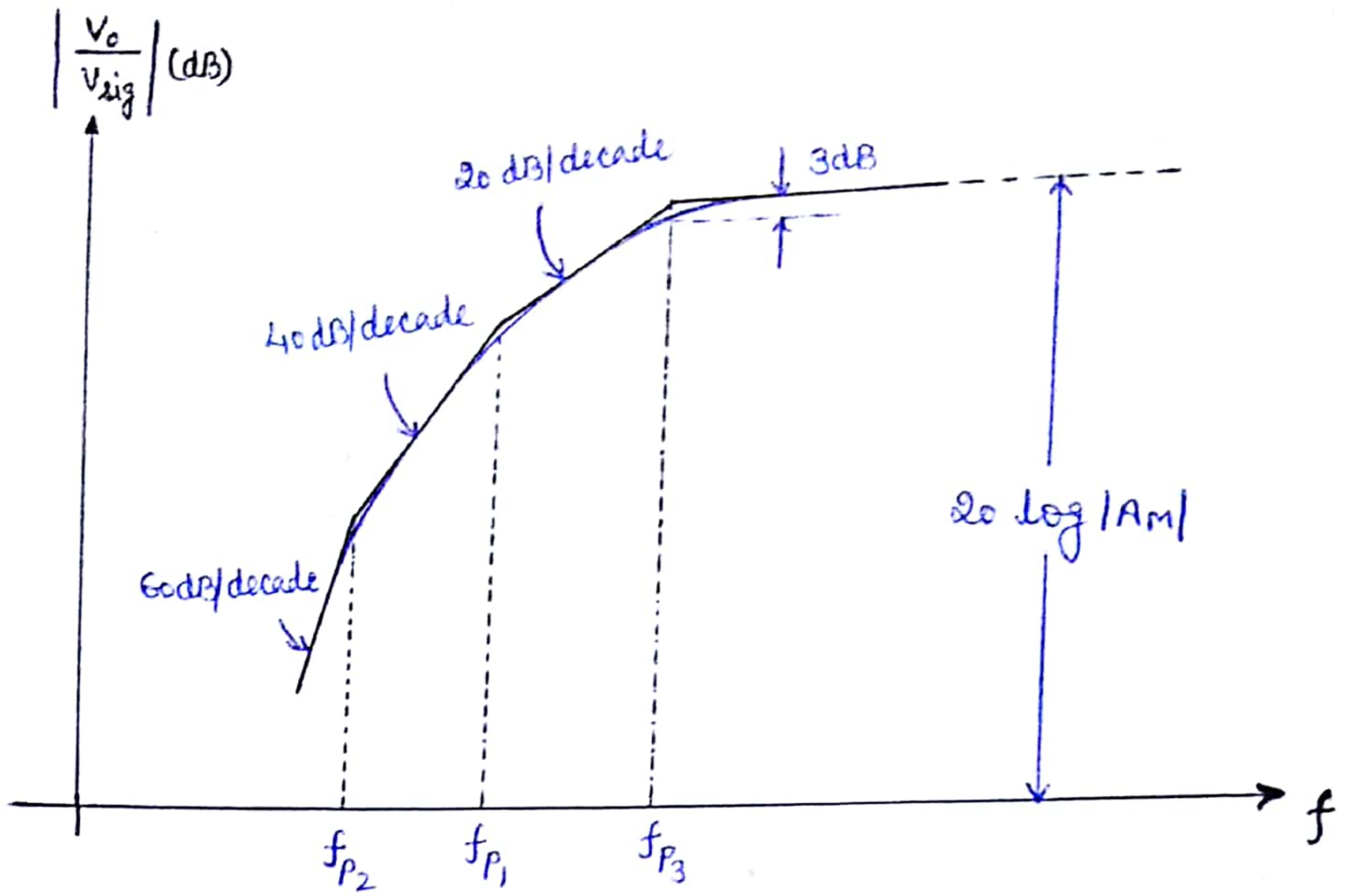


Fig- Freq. Response of CS-amplifier showing all three break frequencies.

For this circuit the largest 3-dB freq. among all three determines the lower 3-dB freq. f_L.

Here in this case $f_{P_2} < f_{P_1} < f_{P_3}$

So $\boxed{f_{P_3} \simeq f_L}$ ⟶ dominant freq.